ANALOG-DIGITAL CONVERSION

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CHAPTER 9
HARDWARE DESIGN TECHNIQUES

This chapter, one of the longer of those within the book, deals with topics just as important as all of those basic circuits immediately surrounding the data converter, discussed earlier. The chapter deals with various and sundry circuit/system issues which fall under the guise of system *hardware design techniques*. In this context, the design techniques may be all those support items surrounding a data converter, excluding the data converter itself. This includes issues of passive components, printed circuit design, power supply systems, protection of linear devices against overvoltage and thermal effects, EMI/RFI issues, high speed logic considerations, and finally, simulation, breadboarding and prototyping. Some of these topics aren't directly involved in the actual signal path of a design, but they are every bit as important as choosing the correct device and surrounding circuit values.

Remote sensing and signal conditioning is such a vital part of data conversion that a considerable amount of discussion is given to topics such as overvoltage protection, cable driving, shielding, and receiving—where the remote interface is often with op amps and instrumentation amplifiers. Much of this material has been extracted from a companion publication by Walter G. Jung: *Op Amp Applications*, Analog Devices, 2002.

SECTION 9.1: PASSIVE COMPONENTS
James Bryant, Walt Jung, Walt Kester

Introduction

When designing with data converters, op amps, and other precision analog devices, it is critical that users avoid the pitfall of poor passive component choice. In fact, the wrong passive component can derail even the best op amp or data converter application. This section includes discussion of some basic traps of choosing passive components for op amp and data converter applications.

So, you've spent good money for a precision op amp or data converter, only to find that, when plugged into your board, the device doesn't meet spec. Perhaps the circuit suffers from drift, poor frequency response, and oscillations—or simply doesn't achieve expected accuracy. Well, before you blame the device, you should closely examine your passive components—including capacitors, resistors, potentiometers, and yes, even the printed circuit boards. In these areas, subtle effects of tolerance, temperature, parasitics, aging, and user assembly procedures can unwittingly sink your circuit. And all too often these effects go unspecified (or underspecified) by passive component manufacturers.

In general, if you use data converters having 12 bits or more of resolution, or op amps that cost more than a few dollars, pay very close attention to passive components.

Consider the case of a 12-bit DAC, where ½ LSB corresponds to 0.012% of full scale, or only 122 ppm. A host of passive component phenomena can accumulate errors far exceeding this! But, buying the most expensive passive components won't necessarily solve your problems either. Often, a *correct* 25-cent capacitor yields a better-performing, more cost-effective design than a premium-grade part. With a few basics, understanding and analyzing passive components may prove rewarding, albeit not easy.

Capacitors

Most designers are generally familiar with the range of capacitors available. But the mechanisms by which both static and dynamic errors can occur in precision circuit designs using capacitors are sometimes easy to forget, because of the tremendous variety of types available. These include dielectrics of glass, aluminum foil, solid tantalum and tantalum foil, silver mica, ceramic, Teflon, and the film capacitors, including polyester, polycarbonate, polystyrene, and polypropylene types. In addition to the traditional leaded packages, many of these are now also offered in surface mount styles.

Figure 9.1 is a workable model of a non-ideal capacitor. The nominal capacitance, C, is shunted by a resistance R_P, which represents *insulation resistance* or leakage. A second resistance, R_S—*equivalent series resistance*, or ESR,—appears in series with the capacitor and represents the resistance of the capacitor leads and plates.

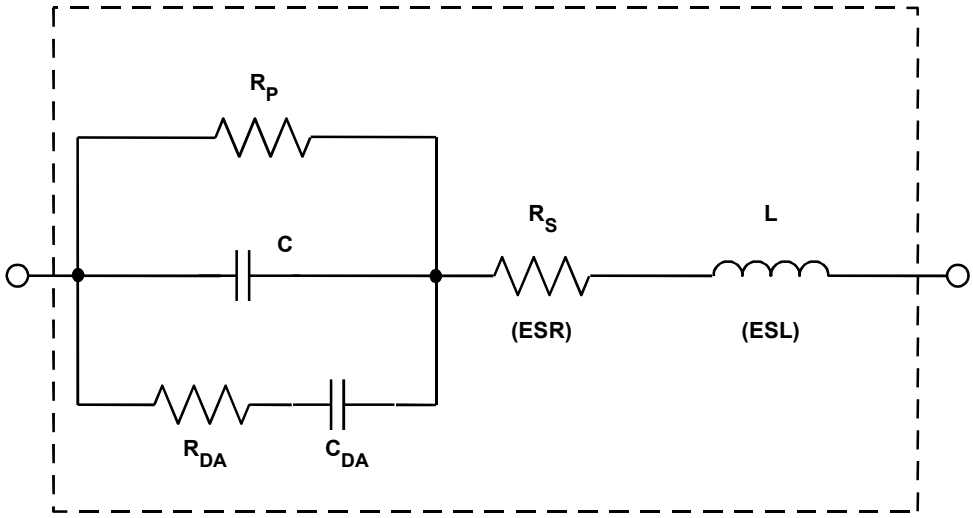


Figure 9.1: *A Non-Ideal Capacitor Equivalent Circuit Includes Parasitic Elements*

Note that capacitor phenomena aren't that easy to isolate. The matching of phenomena and models is for convenience in explanation. Inductance, L—the *equivalent series inductance*, or ESL—models the inductance of the leads and plates. Finally, resistance R_{DA} and capacitance C_{DA} together form a simplified model of a phenomenon known as *dielectric absorption,* or DA. It can ruin fast and slow circuit dynamic performance. In a real capacitor R_{DA} and C_{DA} extend to include multiple parallel sets. These parasitic RC elements can act to degrade timing circuits substantially, and the phenomenon is discussed further below.

Dielectric Absorption

Dielectric absorption, which is also known as "soakage" and sometimes as "dielectric hysteresis"—is perhaps the least understood and potentially most damaging of various capacitor parasitic effects. Upon discharge, most capacitors are reluctant to give up all of their former charge, due to this memory consequence.

Figure 9.2 illustrates this effect. On the left of the diagram, after being charged to the source potential of V volts at time t_o, the capacitor is shorted by the switch S1 at time t_1, discharging it. At time t_2, the capacitor is then open-circuited; a residual voltage slowly builds up across its terminals and reaches a nearly constant value. This error voltage is due to DA, and is shown in the right figure, a time/voltage representation of the charge/discharge/recovery sequence. Note that the recovered voltage error is proportional to both the original charging voltage V, as well as the rated DA for the capacitor in use.

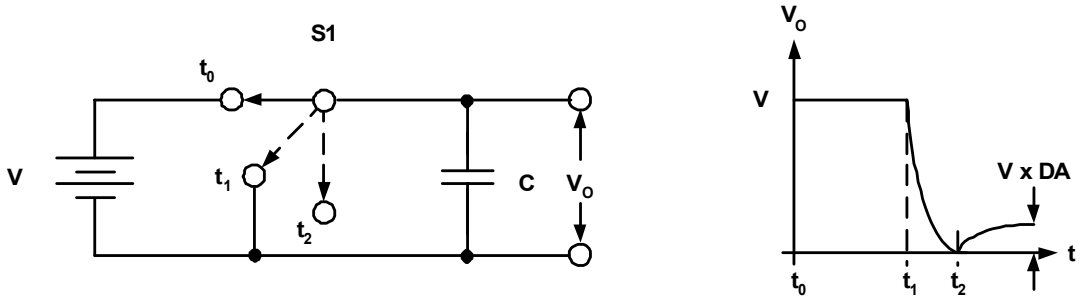


Figure 9.2: *A Residual Open-Circuit Voltage After Charge/Discharge Characterizes Capacitor Dielectric Absorption*

Standard techniques for specifying or measuring dielectric absorption are few and far between. Measured results are usually expressed as the percentage of the original charging voltage that reappears across the capacitor. Typically, the capacitor is charged for a long period, then shorted for a shorter established time. The capacitor is then allowed to recover for a specified period, and the residual voltage is then measured (see Reference 8 for details). While this explanation describes the basic phenomenon, it is important to note that real-world capacitors vary quite widely in their susceptibility to this error, with their rated DA ranging from well below to above 1%, the exact number being a function of the dielectric material used.

In practice, DA makes itself known in a variety of ways. Perhaps an integrator refuses to reset to zero, a voltage-to-frequency converter exhibits unexpected nonlinearity, or a sample-hold amplifier (SHA) exhibits varying errors. This last manifestation can be particularly damaging in a data-acquisition system, where adjacent channels may be at voltages which differ by nearly full scale, as shown below.

Figure 9.3 illustrates the case of DA error in a simple SHA. On the left, switches S1 and S2 represent an input multiplexer and SHA switch, respectively. The multiplexer output voltage is V_X, and the sampled voltage held on C is V_Y, which is buffered by the op amp for presentation to an ADC. As can be noted by the timing diagram on the right, a DA error voltage, ϵ, appears in the hold mode, when the capacitor is effectively open circuit.

This voltage is proportional to the difference of voltages V1 and V2, which, if at opposite extremes of the dynamic range, exacerbates the error. As a practical matter, the best solution for good performance in terms of DA in a SHA is to use only the best capacitor.

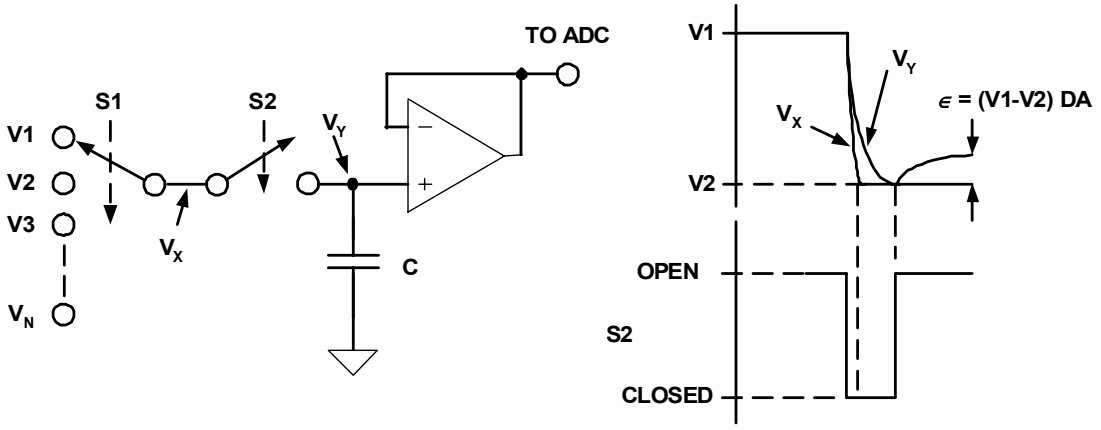


Figure 9.3: *Dielectric Absorption Induces Errors in SHA Applications*

The DA phenomenon is a characteristic of the dielectric material itself, although inferior manufacturing processes or electrode materials can also affect it. DA is specified as a percentage of the charging voltage. It can range from a low of 0.02% for Teflon, polystyrene, and polypropylene capacitors, up to a high of 10% or more for some electrolytics. For some time frames, the DA of polystyrene can be as low as 0.002%.

Common high-K ceramics and polycarbonate capacitor types display typical DA on the order of 0.2%, it should be noted this corresponds to ½ LSB at only 8 bits! Silver mica, glass, and tantalum capacitors typically exhibit even larger DA, ranging from 1.0% to 5.0%, with those of polyester devices falling in the vicinity of 0.5%. As a rule, if the capacitor spec sheet doesn't specifically discuss DA *within your time frame and voltage range*, exercise caution! Another type with lower *specified* DA is likely a better choice.

DA can produce long tails in the transient response of fast-settling circuits, such as those found in high-pass active filters or ac amplifiers. In some devices used for such applications, Figure 9.1's R_{DA}-C_{DA} model of DA can have a time constant of milliseconds. Much longer time constants are also quite usual. In fact, several paralleled R_{DA}-C_{DA} circuit sections with a wide range of time constants can model some devices. In fast-charge, fast-discharge applications, the behavior of the DA mechanism resembles "analog memory"; the capacitor in effect tries to remember its previous voltage.

In some designs, you can compensate for the effects of DA if it is simple and easily characterized, and you are willing to do custom tweaking. In an integrator, for instance, the output signal can be fed back through a suitable compensation network, tailored to cancel the circuit equivalent of the DA by placing a negative impedance effectively in parallel. Such compensation has been shown to improve SH circuit performance by factors of 10 or more (Reference 6).

Capacitor Parasitics and Dissipation Factor

In Figure 9.1, a capacitor's leakage resistance, R_P, the effective series resistance, R_S, and effective series inductance, L, act as parasitic elements, which can degrade an external circuit's performance. The effects of these elements are often lumped together and defined as a dissipation factor, or DF.

A capacitor's leakage is the small current that flows through the dielectric when a voltage is applied. Although modeled as a simple insulation resistance (R_P) in parallel with the capacitor, the leakage actually is nonlinear with voltage. Manufacturers often specify leakage as a megohm-microfarad product, which describes the dielectric's self-discharge time constant, in seconds. It ranges from a low of 1 second or less for high-leakage capacitors, such as electrolytic devices, to the 100s of seconds for ceramic capacitors. Glass devices exhibit self-discharge time-constants of 1,000 or more; but the best leakage performance is shown by Teflon and the film devices (polystyrene, polypropylene), with time constants exceeding 1,000,000 megohm-microfarads. For such a device, external leakage paths—created by surface contamination of the device's case or in the associated wiring or physical assembly—can overshadow the internal dielectric-related leakage.

Effective series inductance, ESL (Figure 9.1, again) arises from the inductance of the capacitor leads and plates, which, particularly at the higher frequencies, can turn a capacitor's normally capacitive reactance into an inductive reactance. Its magnitude strongly depends on construction details within the capacitor. Tubular wrapped-foil devices display significantly more lead inductance than molded radial-lead configurations. Multilayer ceramic (MLC) and film-type devices typically exhibit the lowest series inductance, while ordinary tantalum and aluminum electrolytics typically exhibit the highest. Consequently, standard electrolytic types, if used alone, usually prove insufficient for *high-speed* local bypassing applications. Note however that there also are more specialized aluminum and tantalum electrolytics available, which may be suitable for higher speed uses, however, localized bypassing is still recommended. These are the types generally designed for use in switch-mode power supplies, which are covered more completely in a following section.

Manufacturers of capacitors often specify effective series impedance by means of impedance-versus-frequency plots. Not surprisingly, these curves show graphically a predominantly capacitive reactance at low frequencies, with rising impedance at higher frequencies because of the effect of series inductance.

Effective series resistance, ESR (resistor R_S of Figure 9.1), is made up of the resistance of the leads and plates. As noted, many manufacturers lump the effects of ESR, ESL, and leakage into a single parameter called *dissipation factor*, or DF. Dissipation factor measures the basic inefficiency of the capacitor. Manufacturers define it as the ratio of the energy lost to energy stored per cycle by the capacitor. The ratio of ESR to total capacitive reactance—at a specified frequency—approximates the dissipation factor, which turns out to be equivalent to the reciprocal of the figure of merit, Q. Stated as an approximation, $Q \approx 1/DF$ (with DF in numeric terms). For example, a DF of 0.1% is equivalent to a fraction of 0.001; thus the inverse in terms of Q would be 1000.

Dissipation factor often varies as a function of both temperature and frequency. Capacitors with mica and glass dielectrics generally have DF values from 0.03% to 1.0%. For ceramic devices, DF ranges from a low of 0.1 % to as high as 2.5% at room temperature. And electrolytics usually exceed even this level. The film capacitors are the best as a group, with DFs of less than 0.1 %. Stable-dielectric ceramics, notably the NP0 (also called COG) types, have DF specs comparable to films (more below).

Tolerance, Temperature, and Other Effects

In general, precision capacitors are expensive and—even then—not necessarily easy to buy. In fact, choice of capacitance is limited both by the range of available values, and also by tolerances. In terms of size, the better performing capacitors in the film families tend to be limited in practical terms to 10 μF or less (for dual reasons of size and expense). In terms of low value tolerance, ±1% is possible for NP0 ceramic and some film devices, but with possibly unacceptable delivery times. Many film capacitors can be made available with tolerances of less than ±1%, but on a special order basis only.
Most capacitors are sensitive to temperature variations. DF, DA, and capacitance value are all functions of temperature. For some capacitors, these parameters vary approximately linearly with temperature, in others they vary quite nonlinearly. Although it is usually not important for SHA applications, an excessively large *temperature coefficient* (TC, measured in ppm/°C) can prove harmful to the performance of precision integrators, voltage-to-frequency converters, and oscillators. NP0 ceramic capacitors, with TCs as low as 30 ppm/°C, are the best for stability, with polystyrene and polypropylene next best, with TCs in the 100-200 ppm/°C range. On the other hand, when capacitance stability is important, one should stay away from types with TCs of more than a few hundred ppm/°C, or in fact any TC which is nonlinear.

A capacitor's maximum working temperature should also be considered, in light of the expected environment. Polystyrene capacitors, for instance, melt near 85°C, compared to Teflon's ability to survive temperatures up to 200°C.

Sensitivity of capacitance and DA to applied voltage, expressed as *voltage coefficient*, can also hurt capacitor performance within a circuit application. Although capacitor manufacturers don't always clearly specify voltage coefficients, the user should always consider the possible effects of such factors. For instance, when maximum voltages are applied, some high-K ceramic devices can experience a decrease in capacitance of 50% or more. This is an inherent distortion producer, making such types unsuitable for signal path filtering, for example, and better suited for supply bypassing. Interestingly, NP0 ceramics, the stable dielectric subset from the wide range of available ceramics, do offer good performance with respect to voltage coefficient.

Similarly, the capacitance and dissipation factor of many types vary significantly with frequency, mainly as a result of a variation in dielectric constant. In this regard, the better dielectrics are polystyrene, polypropylene, and Teflon.

Assemble Critical Components Last

The designer's worries don't end with the design process. Some common printed circuit assembly techniques can prove ruinous to even the best designs. For instance, some commonly used cleaning solvents can infiltrate certain electrolytic capacitors—those with rubber end caps are particularly susceptible. Even worse, some of the film capacitors, polystyrene in particular, actually melt when contacted by some solvents. Rough handling of the leads can damage still other capacitors, creating random or even intermittent circuit problems. Etched-foil types are particularly delicate in this regard. To avoid these difficulties it may be advisable to mount especially critical components as the last step in the board assembly process—if possible.

Table 9.1 summarizes selection criteria for various capacitor types, arranged roughly in order of decreasing DA performance. In a selection process, the general information of this table should be supplemented by consultation of current vendor's catalog information (see References at end of section).

Designers should also consider the natural failure mechanisms of capacitors. Metallized film devices, for instance, often self-heal. They initially fail due to conductive bridges that develop through small perforations in the dielectric film. But, the resulting fault currents can generate sufficient heat to destroy the bridge, thus returning the capacitor to normal operation (at a slightly lower capacitance). Of course, applications in high-impedance circuits may not develop sufficient current to clear the bridge, so the designer must be wary here.

Tantalum capacitors also exhibit a degree of self-healing, but—unlike film capacitors—the phenomenon depends on the temperature at the fault location rising slowly. Therefore, tantalum capacitors self-heal best in high impedance circuits which limit the surge in current through the capacitor's defect. Use caution therefore, when specifying tantalums for high-current applications.

Electrolytic capacitor life often depends on the rate at which capacitor fluids seep through end caps. Epoxy end seals perform better than rubber seals, but an epoxy sealed capacitor can explode under severe reverse-voltage or overvoltage conditions. Finally, *all* polarized capacitors must be protected from exposure to voltages outside their specifications.

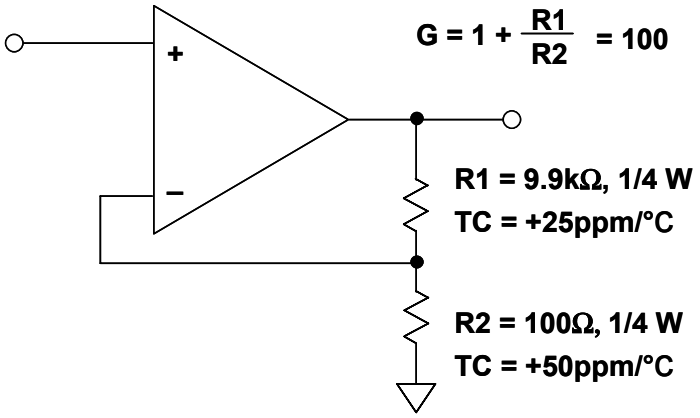
Table 9.1
Capacitor Comparison Chart

TYPE	TYPICAL DA	ADVANTAGES	DISADVANTAGES
Polystyrene	0.001% to 0.02%	Inexpensive Low DA Good stability (~120ppm/°C)	Damaged by temperature > +85°C Large High inductance Vendors limited
Polypropylene	0.001% to 0.02%	Inexpensive Low DA Stable (~200ppm/°C) Wide range of values	Damaged by temperature > +105°C Large High inductance
Teflon	0.003% to 0.02%	Low DA available Good stability Operational above +125 °C Wide range of values	Expensive Large High inductance
Polycarbonate	0.1%	Good stability Low cost Wide temperature range Wide range of values	Large DA limits to 8-bit applications High inductance
Polyester	0.3% to 0.5%	Moderate stability Low cost Wide temperature range Low inductance (stacked film)	Large DA limits to 8-bit applications High inductance (conventional)
NP0 Ceramic	<0.1%	Small case size Inexpensive, many vendors Good stability (30ppm/°C) 1% values available Low inductance (chip)	DA generally low (may not be specified) Low maximum values (≤ 10nF)
Monolithic Ceramic (High K)	>0.2%	Low inductance (chip) Wide range of values	Poor stability Poor DA High voltage coefficient
Mica	>0.003%	Low loss at HF Low inductance Good stability 1% values available	Quite large Low maximum values (≤ 10nF) Expensive
Aluminum Electrolytic	Very high	Large values High currents High voltages Small size	High leakage Usually polarized Poor stability, accuracy Inductive
Tantalum Electrolytic	Very high	Small size Large values Medium inductance	High leakage Usually polarized Expensive Poor stability, accuracy

Resistors and Potentiometers

Designers have a broad range of resistor technologies to choose from, including carbon composition, carbon film, bulk metal, metal film, and both inductive and non-inductive wire-wound types. As perhaps the most basic—and presumably most trouble-free—of components, resistors are often overlooked as error sources in high performance circuits.

Yet, an improperly selected resistor can subvert the accuracy of a 12-bit design by developing errors well in excess of 122 ppm (½ LSB). When did you last read a resistor data sheet? You'd be surprised what can be learned from an informed review of data.



- **Temperature change of 10°C causes gain change of 250ppm**
- **This is 1LSB in a 12-bit system and a disaster in a 16-bit system**

Figure 9.4: *Mismatched Resistor TCs Can Induce Temperature-Related Gain Errors*

Consider the simple circuit of Figure 9.4, showing a non-inverting op amp where the 100× gain is set by R1 and R2. The TCs of these two resistors are a somewhat obvious source of error. Assume the op amp gain errors to be negligible, and that the resistors are perfectly matched to a 99/1 ratio at +25ºC. If, as noted, the resistor TCs differ by only 25 ppm/ºC, the gain of the amplifier changes by 250 ppm for a 10ºC temperature change. This is about a 1 LSB error in a 12-bit system, and a major disaster in a 16-bit system. Temperature changes, however, can limit the accuracy of the Figure 9.4 amplifier in several ways. In this circuit (as well as many op amp circuits with component-ratio defined gains), the *absolute* TC of the resistors is less important—*as long as they track one another in ratio*. But even so, some resistor types simply aren't suitable for precise work. For example, *carbon composition* units—with TCs of approximately 1,500 ppm/°C, won't work. Even if the TCs could be matched to an unlikely 1%, the resulting 15-ppm/°C differential still proves inadequate—an 8°C shift creates a 120-ppm error.

Many manufacturers offer metal film and bulk metal resistors, with absolute TCs ranging between ±1 and ±100 ppm/°C. Beware, though; TCs can vary a great deal, particularly

among discrete resistors from different batches. To avoid this problem, more expensive matched resistor pairs are offered by some manufacturers, with temperature coefficients that track one another to within 2 to 10 ppm/°C. Low-priced thin-film networks have good relative performance and are widely used.

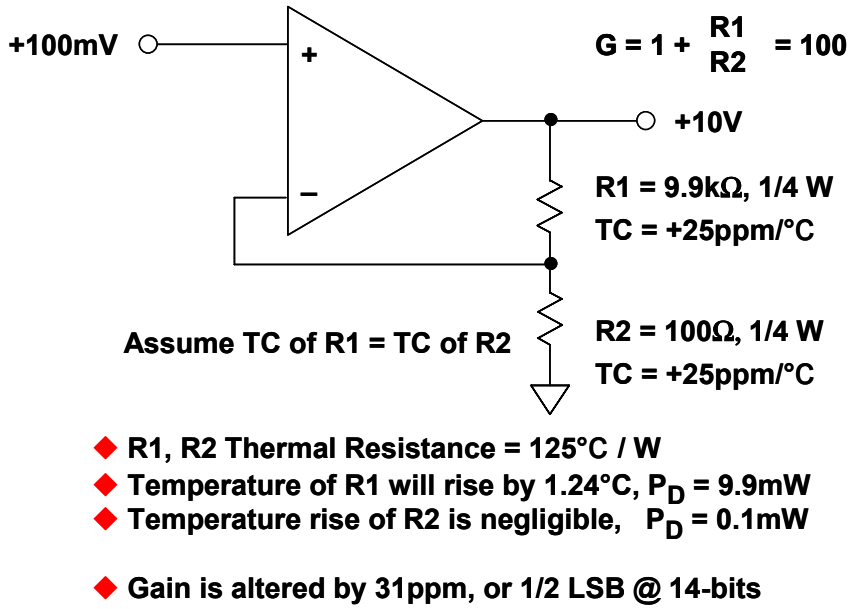


Figure 9.5: *Uneven Power Dissipation Between Resistors With Identical TCs Can Also Introduce Temperature-Related Gain Errors*

Suppose, as shown in Figure 9.5, R1 and R2 are ¼W resistors with identical 25-ppm/ºC TCs. Even when the TCs are identical, there can still be significant errors! When the signal input is zero, the resistors dissipate no heat. But, if it is 100 mV, there is 9.9 V across R1, which then dissipates 9.9 mW. It will experience a temperature rise of 1.24ºC (due to a 125ºC/W, ¼W resistor thermal resistance). This 1.24ºC rise causes a resistance change of 31 ppm, and thus a corresponding gain change. But R2, with only 100 mV across it, is only heated a negligible 0.0125ºC. The resulting 31-ppm net gain error represents a fullscale error of ½ LSB at 14-bits, and is a disaster for a 16-bit system.

Even worse, the effects of this resistor self-heating also create easily calculable *nonlinearity errors*. In the Figure 9.5 example, with ½ the voltage input, the resulting self-heating error is only 15 ppm. In other words, the stage gain is not constant at ½ and full-scale (nor is it so at other points), as long as uneven temperature shifts exist between the gain-determining resistors. This is by no means a worst-case example; physically smaller resistors would give worse results, due to higher associated thermal resistance.

These, and similar errors, are avoided by selecting critical resistors that are accurately matched for both value and TC, are well derated for power, and have tight thermal coupling between those resistors were matching is important. This is best achieved by using a resistor network on a single substrate—such a network may either be within an IC, or it may be a separately packaged thin-film resistor network.

When the circuit resistances are very low (≤10 Ω), *interconnection stability* also becomes important. For example, while often overlooked as an error, the resistance TC of typical copper wire or printed circuit traces can add errors. The TC of copper is typically ~3,900 ppm/°C. Thus a precision 10-Ω, 10-ppm/°C wirewound resistor with 0.1 Ω of copper interconnect effectively becomes a 10.1-Ω resistor with a TC of nearly 50 ppm/°C.

One final consideration applies mainly to designs that see widely varying ambient temperatures: a phenomenon known as *temperature retrace* describes the change in resistance which occurs after a specified number of cycles of exposure to low and high ambients with constant internal dissipation. Temperature retrace can exceed 10 ppm/°C, even for some of the better thin-film components.

In summary, to design resistance-based circuits for minimum temperature-related errors, consider the points noted in Figure 9.6 (along with their cost).

- **Closely match resistance TCs.**
- **Use resistors with low absolute TCs.**
- **Use resistors with low thermal resistance (higher power ratings, larger cases).**
- **Tightly couple matched resistors thermally (use standard common-substrate networks).**
- **For large ratios consider using stepped attenuators.**

Figure 9.6: *A Number of Points are Important Towards Minimizing Temperature-Related Errors in Resistors*

Resistor Parasitics

Resistors can exhibit significant levels of parasitic inductance or capacitance, especially at high frequencies. Manufacturers often specify these parasitic effects as a reactance error, in % or ppm, based on the ratio of the difference between the impedance magnitude and the dc resistance, to the resistance, at one or more frequencies.

Wirewound resistors are especially susceptible to difficulties. Although resistor manufacturers offer wirewound components in either normal or noninductively wound form, even noninductively wound resistors create headaches for designers. These resistors still appear slightly inductive (of the order of 20 µH) for values below 10 kΩ. Above 10 kΩ the same style resistors actually exhibit 5 pF of shunt capacitance.

These parasitic effects can raise havoc in dynamic circuit applications. Of particular concern are applications using wirewound resistors with values greater than 10 kΩ. Here it isn't uncommon to see peaking, or even oscillation. These effects become more evident at low-kHz frequency ranges.

Even in low-frequency circuit applications, parasitic effects in wirewound resistors can create difficulties. Exponential settling to 1 ppm may take 20 time constants or more. The parasitic effects associated with wirewound resistors can significantly increase net circuit settling time to beyond the length of the basic time constants.

Unacceptable amounts of parasitic reactance are often found even in resistors that aren't wirewound. For instance, some metal-film types have significant interlead capacitance, which shows up at high frequencies. In contrast, when considering this end-to-end capacitance, carbon resistors do the best at high frequencies.

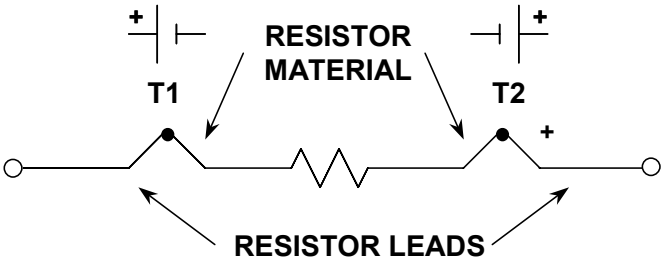
Thermoelectric Effects

Another more subtle problem with resistors is the *thermocouple effect*, also sometimes referred to as *thermal EMF*. Wherever there is a junction between two different metallic conductors, a thermoelectric voltage results. The thermocouple effect is widely used to measure temperature. However, in any low level precision op amp circuit it is also a potential source of inaccuracy, since wherever two different conductors meet, a thermocouple is formed (whether we like it or not). In fact, in many cases, it can easily produce the dominant error within an otherwise precision circuit design.

Parasitic thermocouples will cause errors when and if the various junctions forming the parasitic thermocouples are at different temperatures. With two junctions present on each side of the signal being processed within a circuit, by definition we have formed at least one thermocouple pair. If the two junctions of this thermocouple pair are at different temperatures, there will be a net temperature dependent error voltage produced. Conversely, if the two junctions of a parasitic thermocouple pair are kept at an identical temperature, then the net error produced will be zero, as the voltages of the two thermocouples effectively will be canceled.

This is a critically important point, since in practice we cannot avoid connecting dissimilar metals together to build an electronic circuit. But, what we can do is carefully control temperature differentials across the circuit, so such that the undesired thermocouple errors cancel one another.

The effect of such parasitics is very hard to avoid. To understand this, consider a case of making connections *with copper wire only*. In this case, even a junction formed by different copper wire alloys can have a thermoelectric voltage which is a small fraction of 1 μV/ºC! And, taking things a step further, even such apparently benign components as resistors contain parasitic thermocouples, with potentially even stronger effects.
For example, consider the resistor model shown in Figure 9.7. The two connections between the resistor material and the leads form thermocouple junctions, T1 and T2. This thermocouple EMF can be as high as 400 μV/ºC for some carbon composition resistors, and as low as 0.05 μV/ºC for specially constructed resistors (see Reference 15). Ordinary metal film resistors (RN-types) are typically about 20 μV/ºC.



TYPICAL RESISTOR THERMOCOUPLE EMFs

- **CARBON COMPOSITION** ≈ 400 µV/ °C
- **METAL FILM** ≈ 20 µV/ °C
- **EVENOHM OR MANGANIN WIREWOUND** ≈ 2 µV/ °C
- **RCD Components HP-Series** ≈ 0.05 µV/ °C

Figure 9.7: *Every Resistor Contains Two Thermocouples, Formed Between the Leads and Resistance Element*

Note that these thermocouple effects are relatively unimportant for ac signals. Even for dc-only signals, they will nicely cancel one another, if, as noted above, the entire resistor is at a uniform temperature. However, if there is significant power dissipation in a resistor, or if its orientation with respect to a heat source is non-symmetrical, this can cause one of its ends to be warmer than the other, causing a net thermocouple error voltage. Using ordinary metal film resistors, an end-to-end temperature differential of 1ºC causes a thermocouple voltage of about 20 µV. This error level is quite significant compared to the offset voltage drift of a precision op amp like the OP177, and extremely significant when compared to chopper-stabilized op amps, with their drifts of <1 µV/°C.

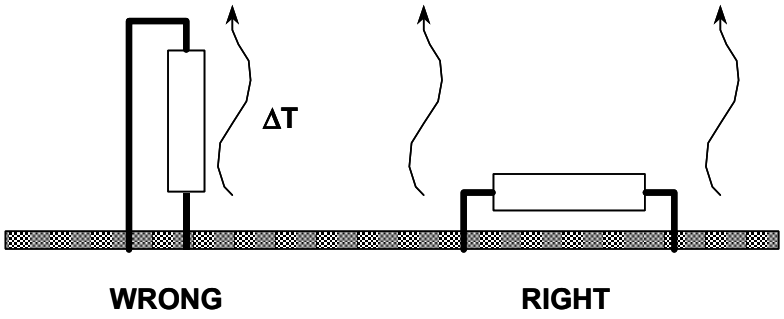


Figure 9.8: *The Effects of Thermocouple EMFs Generated by Resistors can be Minimized by Orientation that Equalizes the End Temperatures*

Figure 9.8 shows how resistor orientation can make a difference in the net thermocouple voltage. In the left diagram, standing the resistor on end in order to conserve board space will invariably cause a temperature gradient across the resistor, especially if it is dissipating any significant power. In contrast, placing the resistor flat on the PC board as shown at the right will generally eliminate the gradient. An exception might occur, if

there is end-to-end resistor airflow. For such cases, orienting the resistor axis perpendicular to the airflow will minimize this source of error, since this tends to force the resistor ends to the same temperature.

Note that this line of thinking should be extended, to include orientation of resistors on a vertically mounted PC board. In such cases, natural convection air currents tend to flow upward across the board. Again, the resistor thermal axis should be perpendicular to convection, to minimize thermocouple effects. With tiny surface mount resistors, the thermocouple effects can be less problematic, due to tighter thermal coupling between the resistor ends.

In general, designers should strive to avoid thermal gradients on or around critical circuit boards. Often this means thermally isolating components that dissipate significant amounts of power. Thermal turbulence created by large temperature gradients can also result in dynamic noise-like low-frequency errors.

Voltage Sensitivity, Failure Mechanisms, and Aging

Resistors are also plagued by changes in value as a function of applied voltage. The deposited-oxide high-megohm type components are especially sensitive, with voltage coefficients ranging from 1 ppm/V to more than 200 ppm/V. This is another reason to exercise caution in such precision applications as high-voltage dividers.

The normal failure mechanism of a resistor can also create circuit difficulties, if not carefully considered beforehand. For example, carbon-composition resistors fail safely, by turning into open circuits. Consequently, in some applications, these components can play a useful secondary role, as a fuse. Replacing such a resistor with a carbon-film type can possibly lead to trouble, since carbon-films can fail as short circuits. (Metal-film components usually fail as open circuits.)

All resistors tend to change slightly in value with age. Manufacturers specify long-term stability in terms of change—ppm/year. Values of 50 or 75 ppm/year are not uncommon among metal film resistors. For critical applications, metal-film devices should be burned-in for at least one week at rated power. During burn-in, resistance values can shift by up to 100 or 200 ppm. Metal film resistors may need 4-5000 operational hours for full stabilization, especially if deprived of a burn-in period.

Resistor Excess Noise

Most designers have some familiarity with thermal, or Johnson noise, which occurs in resistors. But a less widely recognized secondary noise phenomenon is associated with resistors, and it is called *excess noise*. It can prove particularly troublesome in precision op amp and converter circuits, as it is evident only when current passes through a resistor.

To review briefly, thermal noise results from thermally induced random vibration of charge resistor carriers. Although the average current from the vibrations remains zero, instantaneous charge motions result in an instantaneous voltage across the terminals.

Excess noise on the other hand, occurs primarily when dc flows in a discontinuous medium—for example the conductive particles of a carbon composition resistor. The current flows unevenly through the compressed carbon granules, creating microscopic particle-to-particle "arcing". This phenomenon gives rise to a 1/f noise-power spectrum, in addition to the thermal noise spectrum. In other words, the excess spot noise voltage increases as the inverse square-root of frequency.

Excess noise often surprises the unwary designer. Resistor thermal noise and op amp input noise set the noise floor in typical op amp circuits. Only when voltages appear across input resistors and causes current to flow does the excess noise become a significant—and often dominant—factor. In general, carbon composition resistors generate the most excess noise. As the conductive medium becomes more uniform, excess noise becomes less significant. Carbon film resistors do better, with metal film, wirewound and bulk-metal-film resistors doing better yet.

Manufacturers specify excess noise in terms of a noise index—the number of microvolts of rms noise in the resistor in each decade of frequency per volt of dc drop across the resistor. The index can rise to 10 dB (3 microvolts per dc volt per decade of bandwidth) or more. Excess noise is most significant at low frequencies, while above 100 kHz thermal noise predominates.

Potentiometers

Trimming potentiometers (trimpots) can suffer from most of the phenomena that plague fixed resistors. In addition, users must also remain vigilant against some hazards unique to these components.

For instance, many trimpots aren't sealed, and can be severely damaged by board washing solvents, and even by excessive humidity. Vibration—or simply extensive use—can damage the resistive element and wiper terminations. Contact noise, TCs, parasitic effects, and limitations on adjustable range can all hamper trimpot circuit operation. Furthermore, the limited resolution of wirewound types and the hidden limits to resolution in cermet and plastic types (hysteresis, incompatible material TCs, slack) make obtaining and maintaining precise circuit settings anything but an "infinite resolution" process. Given this background, two rules are suggested for the potential trimpot user. Rule 1: Use infinite care and infinitesimal adjustment range to avoid infinite frustration when applying manual trimpots. Rule 2: *Consider the elimination of manual trimming potentiometers altogether, if possible!* A number of digitally addressable potentiometers (RDACs or TrimDACs®) are now available for direct application in similar circuit functions as classic trimpots (See Reference 17). There are also many low cost multi-channel voltage output DACs expressly designed for system voltage trimming.

Table 9.2 summarizes selection criteria for various fixed resistor types, both in discrete form and as part of networks. In a selection process, the general information of this table should be supplemented by consultation of current vendor's catalog information (see References at end of section).

Table 9.2
Resistor Comparison Chart

	TYPE	ADVANTAGES	DISADVANTAGES
DISCRETE	Carbon Composition	Lowest Cost High Power/Small Case Size Wide Range of Values	Poor Tolerance (5%) Poor Temperature Coefficient (1500 ppm/°C)
	Wirewound	Excellent Tolerance (0.01%) Excellent TC (1ppm/°C) High Power	Reactance is a Problem Large Case Size Most Expensive
	Metal Film	Good Tolerance (0.1%) Good TC (<1 to 100ppm/°C) Moderate Cost Wide Range of Values Low Voltage Coefficient	Must be Stabilized with Burn-In Low Power
	Bulk Metal or Metal Foil	Excellent Tolerance (to 0.005%) Excellent TC (to <1ppm/°C) Low Reactance Low Voltage Coefficient	Low Power Very Expensive
	High Megohm	Very High Values (10^8 to $10^{14}\Omega$) Only Choice for Some Circuits	High Voltage Coefficient (200ppm/V) Fragile Glass Case (Needs Special Handling) Expensive
NETWORKS	Thick Film	Low Cost High Power Laser-Trimmable Readily Available	Fair Matching (0.1%) Poor TC (>100ppm/°C) Poor Tracking TC (10ppm/°C)
	Thin Film	Good Matching (<0.01%) Good TC (<100ppm/°C) Good Tracking TC (2ppm/°C) Moderate Cost Laser-Trimmable Low Capacitance Suitable for Hybrid IC Substrate	Often Large Geometry Limited Values and Configurations

Inductance

Stray Inductance

All conductors are inductive, and at high frequencies, the inductance of even quite short pieces of wire or printed circuit traces may be important. The inductance of a straight wire of length L mm and circular cross-section with radius R mm in free space is given by the first equation shown in Figure 9.9.

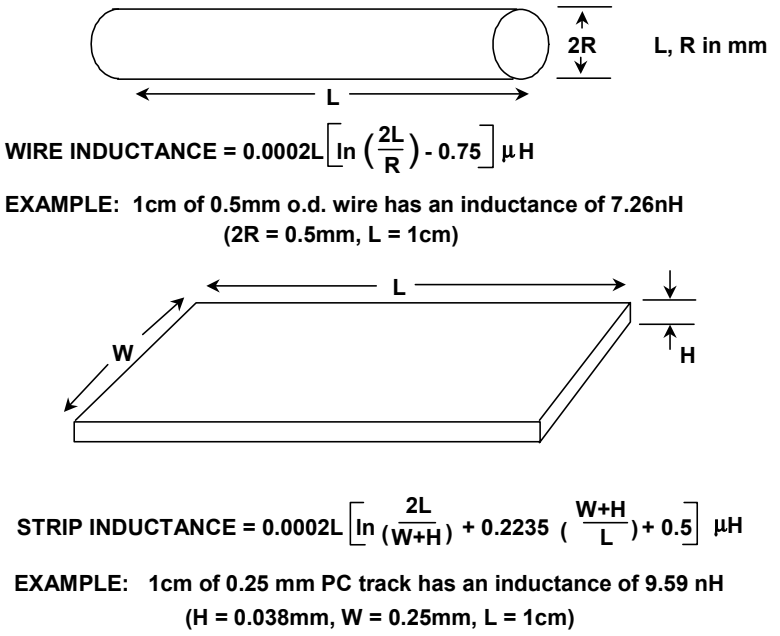


Figure 9.9: *Wire and Strip Inductance Calculations*

The inductance of a strip conductor (an approximation to a PC track) of width W mm and thickness H mm in free space is also given by the second equation in Figure 9.9.

In real systems, both these formulas turn out to be approximate, but they do give some idea of the order of magnitude of inductance involved. They tell us that 1 cm of 0.5-mm od wire has an inductance of 7.26 nH, and 1 cm of 0.25-mm PC track has an inductance of 9.59 nH—these figures are reasonably close to measured results.

At 10 MHz, an inductance of 7.26 nH has an impedance of 0.46 Ω, and so can give rise to 1% error in a 50-Ω system.

Mutual Inductance

Another consideration regarding inductance is the separation of outward and return currents. Kirchoff's Law tells us that current flows in closed paths—there is always an outward and return path. The whole path forms a single-turn inductor.

This principle is illustrated by the contrasting signal trace routing arrangements of Figure 9.10. If the area enclosed within the turn is relatively large, as in the upper "nonideal" picture, then the inductance (and hence the ac impedance) will also be large. On the other

hand, if the outward and return paths are closer together, as in the lower "improved" picture, the inductance will be much smaller.

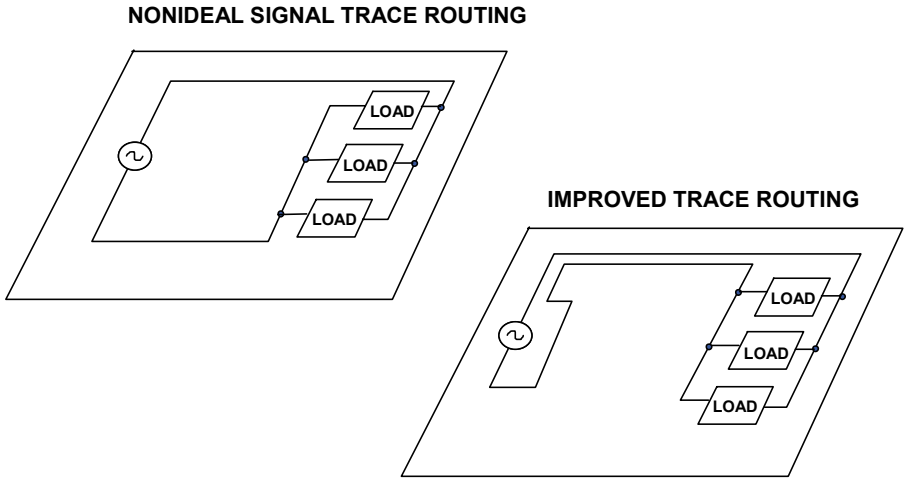
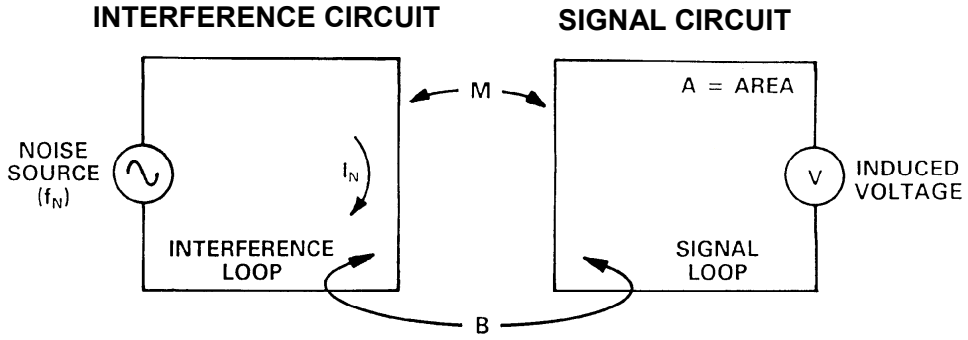


Figure 9.10: *Nonideal and Improved Signal Trace Routing*

Note that the nonideal signal routing case of Figure 9.10 has other drawbacks—the large area enclosed within the conductors produces extensive external magnetic fields, which may interact with other circuits, causing unwanted coupling. Similarly, the large area is more vulnerable to interaction with external magnetic fields, which can induce unwanted signals in the loop.

The basic principle is illustrated in Figure 9.11, and is a common mechanism for the transfer of unwanted signals (noise) between two circuits.



M = MUTUAL INDUCTANCE
B = MAGNETIC REFLUX DENSITY
A = AREA OF SIGNAL LOOP
$\omega_N = 2\pi f_N$ = FREQUENCY OF NOISE SOURCE

V = INDUCED VOLTAGE = $\omega_N M I_N = \omega AB$

Figure 9.11: *Basic Principles of Inductive Coupling*

As with most other noise sources, as soon as we define the working principle, we can see ways of reducing the effect. In this case, reducing any or all of the terms in the equations in Figure 9.11 reduces the coupling. Reducing the frequency or amplitude of the current causing the interference may be impracticable, but it is frequently possible to reduce the mutual inductance between the interfering and interfered with circuits by reducing loop areas on one or both sides and, possibly, increasing the distance between them.

A layout solution is illustrated by Figure 9.12. Here two circuits, shown as Z1 and Z2, are minimized for coupling by keeping each of the loop areas as small as is practical.

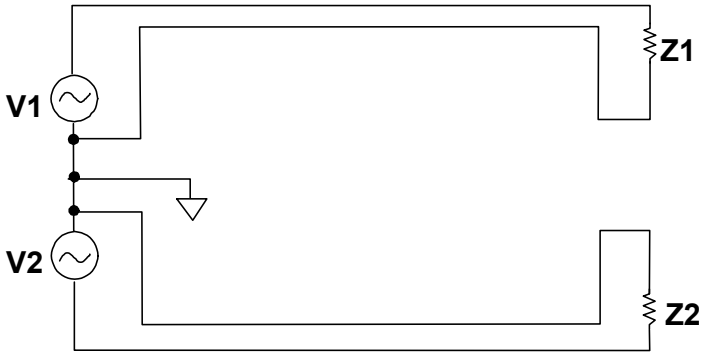


Figure 9.12: *Proper Signal Routing and Layout can Reduce Inductive Coupling*

As also illustrated in Figure 9.13, mutual inductance can be a problem in signals transmitted on cables. Mutual inductance is high in ribbon cables, especially when a single return is common to several signal circuits (top). Separate, dedicated signal and return lines for each signal circuit reduces the problem (middle). Using a cable with twisted pairs for each signal circuit as in the bottom picture is even better.

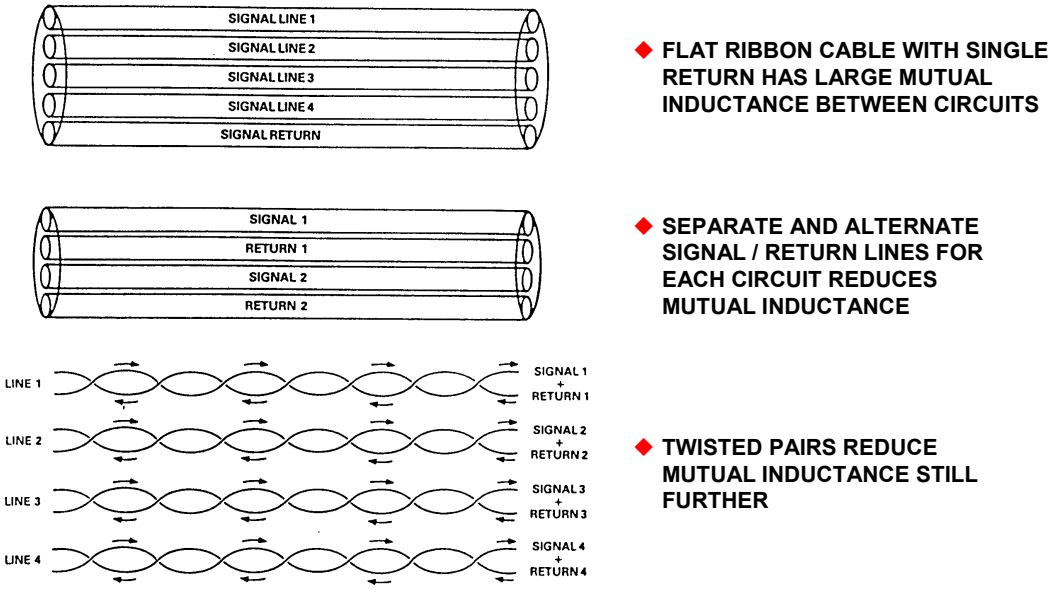


Figure 9.13: *Mutual Inductance and Coupling Within Signal Cabling*

Shielding of magnetic fields to reduce mutual inductance is sometimes possible, but is by no means as easy as shielding an electric field with a Faraday shield (following section). HF magnetic fields are blocked by conductive material provided the skin depth in the conductor at the frequency to be screened is much less than the thickness of the conductor, and the screen has no holes (Faraday shields can tolerate small holes, magnetic screens cannot). LF and dc fields may be screened by a shield made of mu-metal sheet. Mu-metal is an alloy having very high permeability, but it is expensive, its magnetic properties are damaged by mechanical stress, and it will saturate if exposed to too high fields. Its use, therefore, should be avoided where possible.

Ringing

An inductor in series or parallel with a capacitor forms a resonant, or "tuned", circuit, whose key feature is that it shows marked change in impedance over a small range of frequency. Just how sharp the effect is depends on the relative Q of the tuned circuit. The effect is widely used to define the frequency response of narrow-band circuitry, but can also be a potential problem source.

If stray inductance and capacitance (which may or may not be stray) in a circuit should form a tuned circuit, then that tuned circuit may be excited by signals in the circuit, and ring at its resonant frequency.

An example is shown in Figure 9.14, where the resonant circuit formed by an inductive power line and its decoupling capacitor may possibly be excited by fast pulse currents drawn by the powered IC.

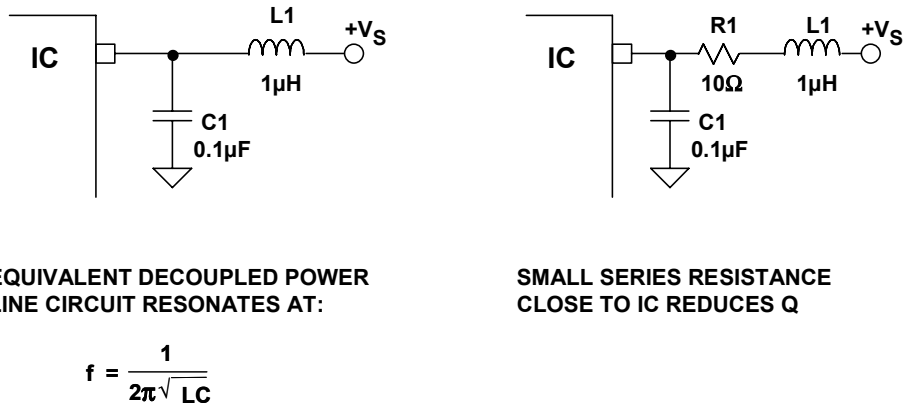


Figure 9.14: *Resonant Circuit Formed by Power Line Decoupling*

While normal trace inductance and typical decoupling capacitances of 0.01-0.1µF will resonate well above a few MHz, an example 0.1-µF capacitor and 1 µH of inductance resonates at 500 kHz. Left unchecked, this could present a resonance problem, as shown in the left case. Should an undesired power line resonance be present, the effect may be minimized by lowering the Q of the inductance. This is most easily done by inserting a small resistance (~10 Ω) in the power line close to the IC, as shown in the right case.

Parasitic Effects in Inductors

Although inductance is one of the fundamental properties of an electronic circuit, inductors are far less common as components than are resistors and capacitors. As for precision components, they are even more rare. This is because they are harder to manufacture, less stable, and less physically robust than resistors and capacitors. It is relatively easy to manufacture stable precision inductors with inductances from nH to tens or hundreds of μH, but larger valued devices tend to be less stable, and large.

As we might expect in these circumstances, circuits are designed, where possible, to avoid the use of precision inductors. We find that stable precision inductors are rarely used in precision analog circuitry, except in tuned circuits for high frequency narrow band applications.

Of course, they are widely used in power filters, switching power supplies and other applications where lack of precision is unimportant (more on this in a following section). The important features of inductors used in such applications are their current carrying and saturation characteristics, and their Q. If an inductor consists of a coil of wire with an air core, its inductance will be essentially unaffected by the current it is carrying. On the other hand, if it is wound on a core of a magnetic material (magnetic alloy or ferrite), its inductance will be non-linear, since at high currents, the core will start to saturate. The effects of such saturation will reduce the efficiency of the circuitry employing the inductor and is liable to increase noise and harmonic generation.

As mentioned above, inductors and capacitors together form tuned circuits. Since all inductors will also have some stray capacity, all inductors will have a resonant frequency (which will normally be published on their data sheet), and should only be used as precision inductors at frequencies well below this.

Q or "Quality Factor"

The other characteristic of inductors is their Q (or "Quality Factor"), which is the ratio of the reactive impedance to the resistance, as indicated in Figure 9.15.

- **$Q = 2\pi f L/R$**
- **The Q of an inductor or resonant circuit is a measure of the ratio of its reactance to its resistance.**
- **The resistance is the HF and NOT the DC value.**
- **The 3 dB bandwidth of a single tuned circuit is Fc/Q where Fc is the center frequency.**

Figure 9.15: *Inductor Q or Quality Factor*

It is rarely possible to calculate the Q of an inductor from its dc resistance, since skin effect (and core losses if the inductor has a magnetic core) ensure that the Q of an inductor at high frequencies is always lower than that predicted from dc values.

Q is also a characteristic of tuned circuits (and of capacitors—but capacitors generally have such high Q values that it may be disregarded, in practice). The Q of a tuned circuit, which is generally very similar to the Q of its inductor (unless it is deliberately lowered by the use of an additional resistor), is a measure of its bandwidth around resonance. LC tuned circuits rarely have Q of much more than 100 (3-dB bandwidth of 1%), but ceramic resonators may have a Q of thousands, and quartz crystals tens of thousands.

Don't Overlook Anything

Remember, if your precision op amp or data-converter-based design does not meet specification, try not to overlook anything in your efforts to find the error sources. Analyze both active *and* passive components, trying to identify and challenge any assumptions or preconceived notions that may blind you to the facts. Take nothing for granted.

For example, when not tied down to prevent motion, cable conductors, moving within their surrounding dielectrics, can create significant static charge buildups that cause errors, especially when connected to high-impedance circuits. Rigid cables, or even costly low-noise Teflon-insulated cables, are expensive alternative solutions.

As more and more high-precision op amps become available, and system designs call for higher speed and increased accuracy, a thorough understanding of the error sources described in this section (as well those following) becomes more important.

Some additional discussions of passive components within a succeeding power supply filtering section complements this one. In addition, the very next section on PCB design issues also complements many points within this section. Similar comments apply to the section on EMI/RFI.

REFERENCES:
9.1 PASSIVE COMPONENTS

1. James E. Buchanan, "Dielectric Absorption— It Can Be a Real Problem In Timing Circuits," **EDN**, January 20, 1977, p 83.

2. Lew Counts and Scott Wurcer, "Instrumentation Amplifier Nears Input Noise Floor," **Electronic Design,** June 10, 1982.

3. W. Doeling, W. Mark, T. Tadewald, and P. Reichenbacher, "Getting Rid of Hook: The Hidden PC-Board Capacitance," **Electronics,** October 12, 1978, p 111-117.

4. Tarlton Fleming, "Data-Acquisition System (DAS) Design Considerations," **WESCON '81 Professional Program Session Record No. 23**.

5. Walter G. Jung and Richard Marsh, "Picking Capacitors, Parts I and II," **Audio**, February and March, 1980.

6. Robert A. Pease, "Understand Capacitor Soakage to Optimize Analog Systems", **EDN**, October 13, 1982, page 125.

7. Andy Rappaport, "Capacitors" **EDN**, October 13, 1982, page 105.

8. Specification MIL-PRF-19978G, Capacitors, Fixed, Plastic (or Paper-Plastic) Dielectric (Hermetically Sealed in Metal, Ceramic or Glass Cases), Established and Non-Established Reliability General Specification for, May 27, 1999.

9. Specification MIL-PRF-123B, Capacitors, Fixed, Ceramic Dielectric, (Temperature Stable and General Purpose), High Reliability, General Specification for, August 6, 1990.

10. **Tantalum and Ceramic Surface Mount Capacitor Catalog**, Kemet Electronics Corporation, P.O. Box 5928, Greenville, SC, 29606, 864-963-6300.

11. A general capacitor information resource: http://www.faradnet.com/

12. Southern and F-Dyne film capacitors, Southern Electronics, 215 Research Drive, Milford, CT, 06460, 203-876-7488.

13. Wesco film capacitors, Wesco Electrical Company, 201 Munson Street, Greenfield, MA, 01301, 413-774-4358.

14. Doug Grant and Scott Wurcer, "Avoiding Passive Component Pitfalls," **The Best of Analog Dialogue**, Analog Devices, 1991, p. 143-148.

15. RCD Components, Inc., 520 E. Industrial Park Drive, Manchester NH, 03109, 603-669-0054, http://www.rcd-comp.com

16. Steve Sockolov and James Wong, "High-Accuracy Analog Needs More Than Op Amps," **Electronic Design**, October 1, 1992, p.53.

17. Selection guide for digital potentiometers: http://www.analog.com/digitalpots

18. Precision Resistor Co., Inc., 10601 75th St. N., Largo, FL, 33777-1427, 727 541-5771, http://www.precisionresistor.com

19. Ohmite Victoreen MAXI-MOX Resistors, 3601 Howard Street, Skokie, IL 60076, 847 675-2600, http://www.ohmite.com/victoreen/.

20. Vishay/Dale Resistors, 2300 Riverside Blvd., Norfolk, NE, 68701-2242, 402 371-0800, http://www.vishay.com.

21. Beyschlag Resistor Products, PO Box 1220, D-25732 Heide, Germany, http://www.beyschlag.com

22. B. I. & B. Bleaney, **Electricity & Magnetism**, Oxford at the Clarendon Press, 1957, pp 23, 24, & 52.

23. Henry W. Ott, **Noise Reduction Techniques in Electronic Systems, 2nd Edition**, John Wiley, Inc., 1988, ISBN: 0-471-85068-3.

24. G. W. A. Dummer, **Materials for Conductive and Resistive Functions**, Hayden, 1970.

Acknowledgements:

Portions of this and the following section were adapted from Doug Grant and Scott Wurcer, "Avoiding Passive Component Pitfalls," originally published in **Analog Dialogue 17-2**, 1983.

SECTION 9.2: PC BOARD DESIGN ISSUES

James Bryant, Walt Kester, Walt Jung

Printed circuit boards (PCBs) are by far the most common method of assembling modern electronic circuits. Comprised of a sandwich of insulating layer (or layers) and one or more copper conductor patterns, they can introduce various forms of errors into a circuit, particularly if the circuit is operating at either high precision or high speed. PCBs then, act as "unseen" components, wherever they are used in precision circuit designs. Since designers don't always consider the PCB electrical characteristics as additional components of their circuit, overall performance can easily end up worse than predicted. This general topic, manifested in many forms, is the focus of this section.

PCB effects that are harmful to precision circuit performance include leakage resistances; spurious voltage drops in trace foils, vias, and ground planes; the influence of stray capacitance, dielectric absorption (DA), and the related "hook." In addition, the tendency of PCBs to absorb atmospheric moisture, *hygroscopicity,* means that changes in humidity often cause the contributions of some parasitic effects to vary from day to day.

In general, PCB effects can be divided into two broad categories— those that most noticeably affect the static or dc operation of the circuit, and those that most noticeably affect dynamic or ac circuit operation.

Another very broad area of PCB design is the topic of grounding. Grounding is a problem area in itself for all analog designs, and it can be said that implementing a PCB based circuit doesn't change that fact. Fortunately, certain principles of quality grounding, namely the use of ground planes, are intrinsic to the PCB environment. This factor is one of the more significant advantages to PCB based analog designs, and an appreciable amount of this section is focused on this issue.

Some other aspects of grounding that must be managed include the control of spurious ground and signal return voltages that can degrade performance. These voltages can be due to external signal coupling, common currents, or simply excessive IR drops in ground conductors. Proper conductor routing and sizing, as well as differential signal handling and ground isolation techniques enables control of such parasitic voltages.

One final area of grounding to be discussed is grounding appropriate for a mixed-signal, analog/digital environment. This topic is the subject of many application calls, and it is certainly true that interfacing with ADCs (or DACs) is a major part of the system design, and thus it shouldn't be overlooked. Indeed, the single issue of quality grounding can drive the entire layout philosophy of a high performance mixed signal PCB design— as it well should.

Resistance of Conductors

Every engineer is familiar with resistors, although perhaps fewer are aware of their idiosyncrasies, as generally covered in Section 9.1. But far too few engineers consider that all the wires and PCB traces with which their systems and circuits are assembled are also resistors. In higher precision systems, even these trace resistances and simple wire interconnections can have degrading effects. Copper is *not* a superconductor—and too many engineers appear to think it is!

Figure 9.16 illustrates a method of calculating the sheet resistance R of a copper square, given the length Z, the width X, and the thickness Y.

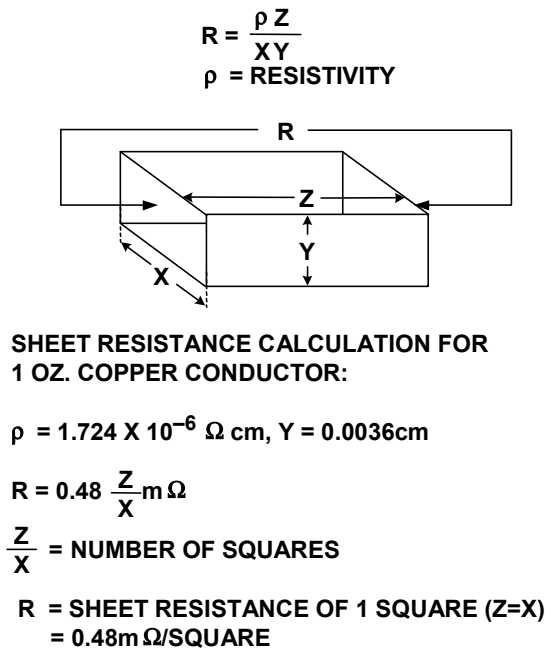


Figure 9.16: *Calculation of Sheet Resistance and Linear Resistance for Standard Copper PCB Conductors*

At 25°C the resistivity of pure copper is 1.724×10^{-6} Ωcm. The thickness of standard 1 ounce PCB copper foil is 0.036 mm (0.0014"). Using the relations shown, the resistance of such a standard copper element is therefore 0.48 mΩ /square. One can readily calculate the resistance of a linear trace, by effectively "stacking" a series of such squares end-end, to make up the line's length. The line length is Z and the width is X, so the line resistance R is simply a product of Z/X and the resistance of a single square, as noted in the figure.

For a given copper weight and trace width, a resistance/length calculation can be made. For example, the 0.25-mm (10-mil) wide traces frequently used in PCB designs equates to a resistance/length of about 19 mΩ/cm (48 mΩ /inch), which is quite large. Moreover, the temperature coefficient of resistance for copper is about 0.4% /°C around room temperature. This is a factor that shouldn't be ignored, in particular within low impedance precision circuits, where the TC can shift the net impedance over temperature.

As shown in Figure 9.17, PCB trace resistance can be a serious error when conditions aren't favorable. Consider a 16-bit ADC with a 5-kΩ input resistance, driven through 5 cm of 0.25-mm wide 1-oz PCB track between it and its signal source. The track resistance of nearly 0.1 Ω forms a divider with the 5-kΩ load, creating an error. The resulting voltage drop is a gain error of 0.1/5000 (~0.0019%), well over 1 LSB (0.0015% for 16 bits).

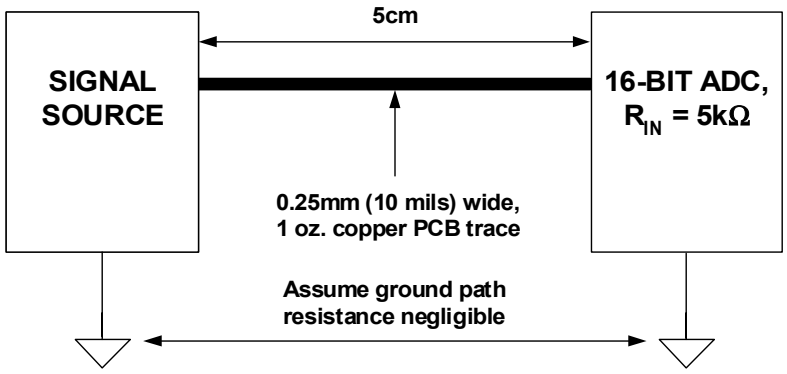


Figure 9.17: *Ohm's Law Predicts >1 LSB of Error due to Drop In PCB Conductor*

So, when dealing with precision circuits, the point is made that even simple design items such as PCB trace resistance cannot be dealt with casually. There are various solutions that can address this issue, such as wider traces (which may take up excessive space), the use of heavier copper (which may be too expensive), or simply choosing a high impedance converter. But, the most important thing is to think it all through, avoiding any tendency to overlook items appearing innocuous on the surface.

Voltage Drop in Signal Leads—"Kelvin" Feedback

The gain error resulting from resistive voltage drop in PCB signal leads is important only with high precision and/or at high resolutions (the Figure 9.17 example), or where large signal currents flow. Where load impedance is constant and resistive, adjusting overall system gain can compensate for the error. In other circumstances, it may often be removed by the use of "Kelvin" or "voltage sensing" feedback, as shown in Figure 9.18.

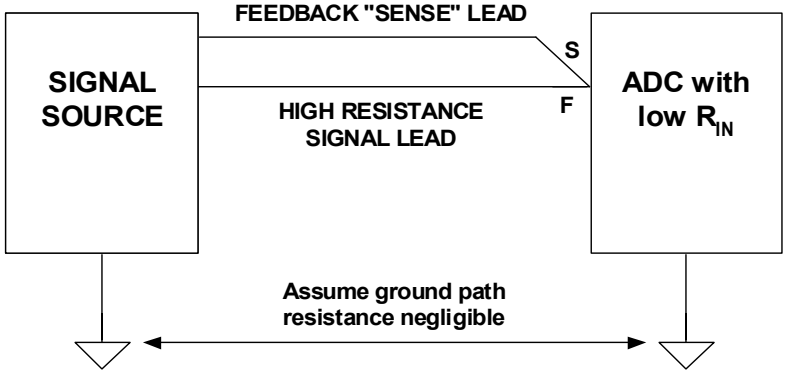


Figure 9.18: *Use of a Sense Connection Moves Accuracy to the Load Point*

In this modification to the case of Figure 9.17, a long resistive PCB trace is still used to drive the input of a high resolution ADC, with low input impedance. In this case however, the voltage drop in the signal lead does *not* give rise to an error, as feedback is taken directly from the input pin of the ADC, and returned to the driving source. This scheme allows full accuracy to be achieved in the signal presented to the ADC, despite any voltage drop across the signal trace.

The use of separate force (F) and sense (S) connections at the load removes any errors resulting from voltage drops in the force lead, but, of course, may only be used in systems where there is negative feedback. It is also impossible to use such an arrangement to drive two or more loads with equal accuracy, since feedback may only be taken from one point. Also, in this much-simplified system, errors in the common lead source/load path are ignored, the assumption being that ground path voltages are negligible. In many systems this may not necessarily be the case, and additional steps may be needed, as noted below.

Signal Return Currents

Kirchoff's Law tells us that at any point in a circuit the algebraic sum of the currents is zero. This tells us that all currents flow in circles and, particularly, that the return current must always be considered when analyzing a circuit, as is illustrated in Figure 9.19 (see References 7 and 8).

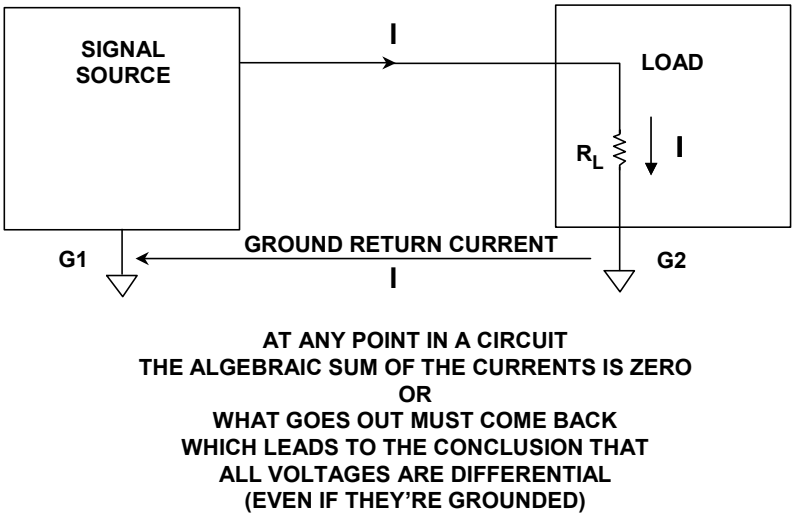


Figure 9.19: *Kirchoff's Law Helps in Analyzing Voltage Drops Around a Complete Source/Load Coupled Circuit*

In dealing with grounding issues, common human tendencies provide some insight into how the correct thinking about the circuit can be helpful towards analysis. Most engineers readily consider the ground return current, "I", *when they are considering a fully differential circuit*.

However, when considering the more usual circuit case, where a single-ended signal is referred to "ground", it is common to assume that all the points on the circuit diagram

where ground symbols are found are at the same potential. Unfortunately, this happy circumstance just ain't necessarily so!

This overly optimistic approach is illustrated in Figure 9.20, where, if it really should exist, "infinite ground conductivity" would lead to zero ground voltage difference between source ground G1 and load ground G2. Unfortunately this approach isn't a wise practice, and when dealing with high precision circuits, it can lead to disasters.

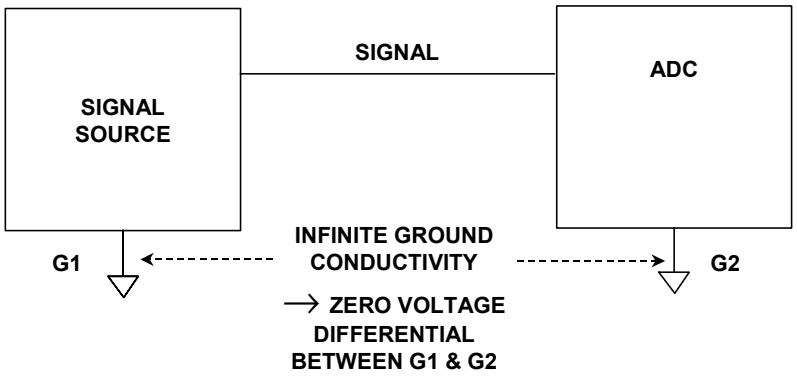


Figure 9.20: *Unlike This Optimistic Diagram, it is Unrealistic to Assume Infinite Conductivity Between Source/Load Grounds in a Real-World System*

A more realistic approach to ground conductor integrity includes analysis of the impedance(s) involved, and careful attention to minimizing spurious noise voltages.

A more realistic model of a ground system is shown in Figure 9.21. The signal return current flows in the complex impedance existing between ground points G1 and G2 as shown, giving rise to a voltage drop ΔV in this path. But it is important to note that additional *external* currents, such as I_{EXT}, may also flow in this same path. It is critical to understand that such currents may generate uncorrelated noise voltages between G1 and G2 (dependent upon the current magnitude and relative ground impedance).

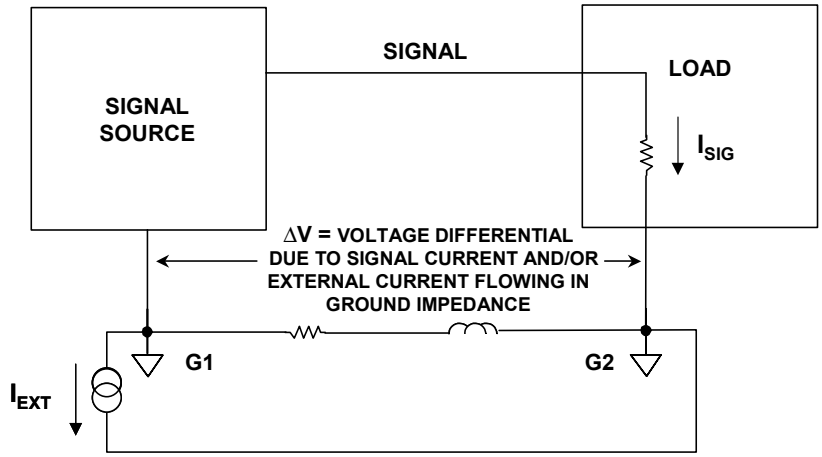


Figure 9.21: *A More Realistic Source-to-Load Grounding System View Includes Consideration of the Impedance Between G1-G2, Plus the Effect of Any Non-Signal-Related Currents*

Some portion of these undesired voltages may end up being seen at the signal's load end, and they can have the potential to corrupt the signal being transmitted.

Grounding in Mixed Analog/Digital Systems

Walt Kester, James Bryant, Mike Byrne

Today's signal processing systems generally require mixed-signal devices such as analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) as well as fast digital signal processors (DSPs). Requirements for processing analog signals having wide dynamic ranges increases the importance of high performance ADCs and DACs. Maintaining wide dynamic range with low noise in hostile digital environments is dependent upon using good high-speed circuit design techniques including proper signal routing, decoupling, and grounding.

In the past, "high precision, low-speed" circuits have generally been viewed differently than so-called "high-speed" circuits. With respect to ADCs and DACs, the sampling (or update) frequency has generally been used as the distinguishing speed criteria. However, the following two examples show that in practice, most of today's signal processing ICs are really "high-speed," and must therefore be treated as such in order to maintain high performance. This is certainly true of DSPs, and also true of ADCs and DACs.

All sampling ADCs (ADCs with an internal sample-and-hold circuit) suitable for signal processing applications operate with relatively high speed clocks with fast rise and fall times (generally a few nanoseconds) and must be treated as high speed devices, even though throughput rates may appear low. For example, a medium-speed 12-bit successive approximation (SAR) ADC may operate on a 10-MHz internal clock, while the sampling rate is only 500 kSPS.

Sigma-delta (Σ-Δ) ADCs also require high speed clocks because of their high oversampling ratios. Even high resolution, so-called "low frequency" Σ-Δ industrial measurement ADCs (having throughputs of 10 Hz to 7.5 kHz) operate on 5-MHz or higher clocks and offer resolution to 24-bits (for example, the Analog Devices AD77xx-series).

To further complicate the issue, mixed-signal ICs have both analog and digital ports, and because of this, much confusion has resulted with respect to proper grounding techniques. In addition, some mixed-signal ICs have relatively low digital currents, while others have high digital currents. In many cases, these two types must be treated differently with respect to optimum grounding.

Digital and analog design engineers tend to view mixed-signal devices from different perspectives, and the purpose of this section is to develop a general grounding philosophy that will work for most mixed signal devices, without having to know the specific details of their internal circuits.

Ground and Power Planes

The importance of maintaining a low impedance large area ground plane is critical to all analog circuits today. The ground plane not only acts as a low impedance return path for

decoupling high frequency currents (caused by fast digital logic) but also minimizes EMI/RFI emissions. Because of the shielding action of the ground plane, the circuit's susceptibility to external EMI/RFI is also reduced.

Ground planes also allow the transmission of high speed digital or analog signals using transmission line techniques (microstrip or stripline) where controlled impedances are required.

The use of "buss wire" is totally unacceptable as a "ground" because of its impedance at the equivalent frequency of most logic transitions. For instance, #22 gauge wire has about 20 nH/inch inductance. A transient current having a slew rate of 10 mA/ns created by a logic signal would develop an unwanted voltage drop of 200 mV at this frequency flowing through 1 inch of this wire:

$$\Delta v = L\frac{\Delta i}{\Delta t} = 20\ \text{nH} \times \frac{10\ \text{mA}}{\text{ns}} = 200\ \text{mV}. \qquad \text{Eq. 9.1}$$

For a signal having a 2-V peak-to-peak range, this translates into an error of about 200 mV, or 10% (approximate 3.5-bit accuracy). Even in all-digital circuits, this error would result in considerable degradation of logic noise margins.

Figure 9.22 shows an illustration of a situation where the digital return current modulates the analog return current (top figure). The ground return wire inductance and resistance is shared between the analog and digital circuits, and this is what causes the interaction and resulting error. A possible solution is to make the digital return current path flow directly to the GND REF as shown in the bottom figure. This is the fundamental concept of a "star," or single-point ground system. Implementing the true single-point ground in a system which contains multiple high frequency return paths is difficult because the physical length of the individual return current wires will introduce parasitic resistance and inductance which can make obtaining a low impedance high frequency ground difficult. In practice, the current returns must consist of large area ground planes for low impedance to high frequency currents. Without a low-impedance ground plane, it is therefore almost impossible to avoid these shared impedances, especially at high frequencies.

All integrated circuit ground pins should be soldered directly to the low-impedance ground plane to minimize series inductance and resistance. The use of traditional IC sockets is not recommended with high-speed devices. The extra inductance and capacitance of even "low profile" sockets may corrupt the device performance by introducing unwanted shared paths. If sockets must be used with DIP packages, as in prototyping, individual "pin sockets" or "cage jacks" may be acceptable. Both capped and uncapped versions of these pin sockets are available (AMP part numbers 5-330808-3, and 5-330808-6). They have spring-loaded gold contacts which make good electrical and mechanical connection to the IC pins. Multiple insertions, however, may degrade their performance.

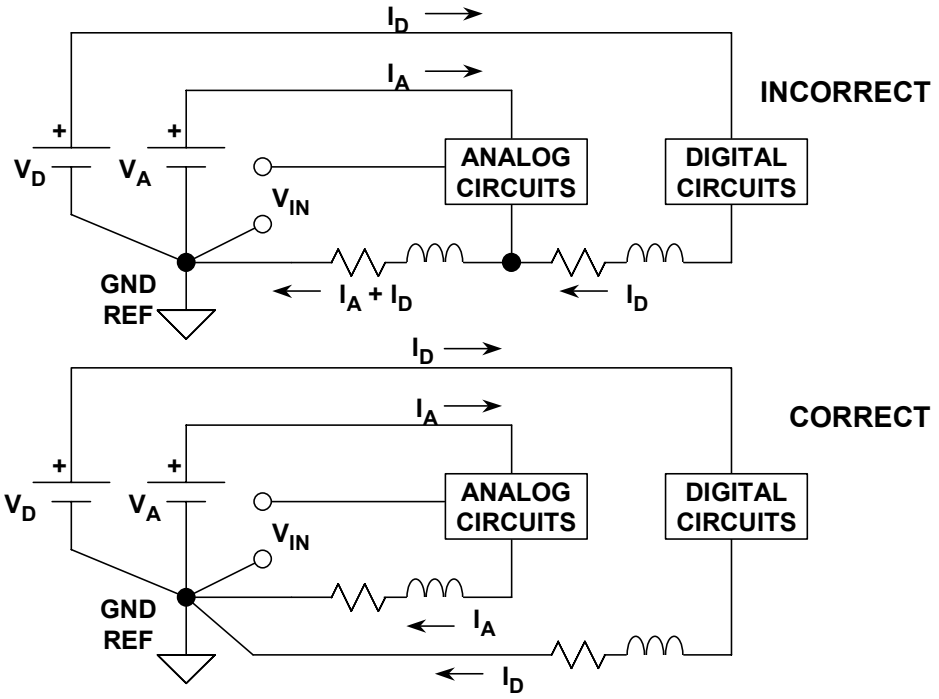


Figure 9.22: *Digital Currents Flowing in Analog Return Path Create Error Voltages*

Power supply pins should be decoupled directly to the ground plane using low inductance ceramic surface mount capacitors. If through-hole mounted ceramic capacitors must be used, their leads should be less than 1 mm. The ceramic capacitors should be located as close as possible to the IC power pins. Ferrite beads may be also required for additional decoupling.

Double-Sided vs. Multilayer Printed Circuit Boards

Each PCB in the system should have at least one complete layer dedicated to the ground plane. Ideally, a double-sided board should have one side completely dedicated to ground and the other side for interconnections. In practice, this is not possible, since some of the ground plane will certainly have to be removed to allow for signal and power crossovers, vias, and through-holes. Nevertheless, as much area as possible should be preserved, and at least 75% should remain. After completing an initial layout, the ground layer should be checked carefully to make sure there are no isolated ground "islands," because IC ground pins located in a ground "island" have no current return path to the ground plane. Also, the ground plane should be checked for "skinny" connections between adjacent large areas which may significantly reduce the effectiveness of the ground plane. Needless to say, auto-routing board layout techniques will generally lead to a layout disaster on a mixed-signal board, so manual intervention is highly recommended.

Systems that are densely packed with surface mount ICs will have a large number of interconnections; therefore multilayer boards are mandatory. This allows at least one complete layer to be dedicated to ground. A simple 4-layer board would have internal ground and power plane layers with the outer two layers used for interconnections

between the surface mount components. Placing the power and ground planes adjacent to each other provides additional inter-plane capacitance which helps high frequency decoupling of the power supply. In most systems, 4-layers are not enough, and additional layers are required for routing signals as well as power. Figure 9.23 summarizes the key issues relating to ground planes.

- **Use Large Area Ground (and Power) Planes for Low Impedance Current Return Paths (Must Use at Least a Double-Sided Board!)**
- **Double-Sided Boards:**
  - **Avoid High-Density Interconnection Crossovers and Vias Which Reduce Ground Plane Area**
  - **Keep > 75% Board Area on One Side for Ground Plane**
- **Multilayer Boards: Mandatory for Dense Systems**
  - **Dedicate at Least One Layer for the Ground Plane**
  - **Dedicate at Least One Layer for the Power Plane**
- **Use at Least 30% to 40% of PCB Connector Pins for Ground**
- **Continue the Ground Plane on the Backplane Motherboard to Power Supply Return**

Figure 9.23: *Ground Planes Are Mandatory!*

Multicard Mixed-Signal Systems

The best way of minimizing ground impedance in a multicard system is to use a "motherboard" PCB as a backplane for interconnections between cards, thus providing a continuous ground plane to the backplane. The PCB connector should have at least 30-40% of its pins devoted to ground, and these pins should be connected to the ground plane on the backplane mother card. To complete the overall system grounding scheme there are two possibilities:

1. The backplane ground plane can be connected to chassis ground at numerous points, thereby diffusing the various ground current return paths. This is commonly referred to as a "multipoint" grounding system and is shown in Figure 9.24.

2. The ground plane can be connected to a single system "star ground" point (generally at the power supply).

The first approach is most often used in all-digital systems, but can be used in mixed-signal systems provided the ground currents due to digital circuits are sufficiently low and diffused over a large area. The low ground impedance is maintained all the way through the PC boards, the backplane, and ultimately the chassis. However, it is critical that good electrical contact be made where the grounds are connected to the sheet metal chassis. This requires self-tapping sheet metal screws or "biting" washers. Special care must be taken where anodized aluminum is used for the chassis material, since its surface acts as an insulator.

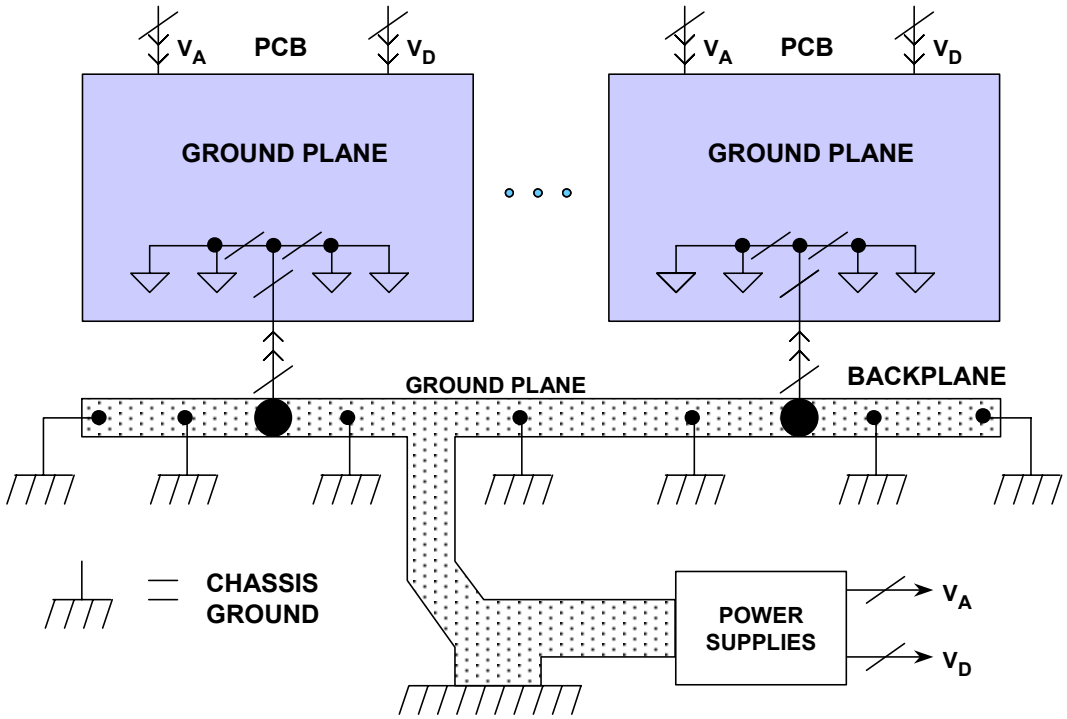


Figure 9.24: *Multipoint Ground Concept*

The second approach ("star ground") is often used in high speed mixed-signal systems having separate analog and digital ground systems and warrants further discussion.

Separating Analog and Digital Grounds

In mixed-signal systems with large amounts of digital circuitry, it is highly desirable to *physically* separate sensitive analog components from noisy digital components. It may also be beneficial to use separate ground planes for the analog and the digital circuitry. These planes should not overlap in order to minimize capacitive coupling between the two. The separate analog and digital ground planes are continued on the backplane using either motherboard ground planes or "ground screens" which are made up of a series of wired interconnections between the connector ground pins. The arrangement shown in Figure 9.25 illustrates that the two planes are kept separate all the way back to a common system "star" ground, generally located at the power supplies. The connections between the ground planes, the power supplies, and the "star" should be made up of multiple bus bars or wide copper braids for minimum resistance and inductance. The back-to-back Schottky diodes on each PCB are inserted to prevent accidental dc voltage from developing between the two ground systems when cards are plugged and unplugged. This voltage should be kept less than 300 mV to prevent damage to ICs which have connections to both the analog and digital ground planes. Schottky diodes are preferable because of their low capacitance and low forward voltage drop. The low capacitance prevents ac coupling between the analog and digital ground planes. Schottky diodes begin to conduct at about 300 mV, and several parallel diodes in parallel may be required if high currents are expected. In some cases, ferrite beads can be used instead of Schottky diodes, however they introduce dc ground loops which can be troublesome in precision systems.

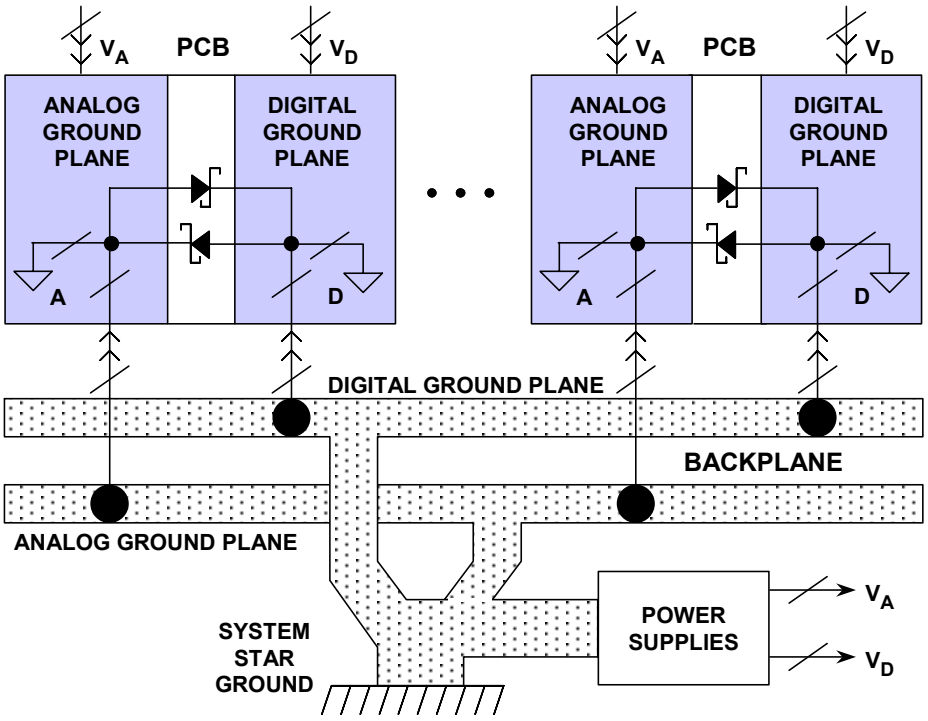


Figure 9.25: *Separating Analog and Digital Ground Planes*

It is mandatory that the impedance of the ground planes be kept as low as possible, all the way back to the system star ground. DC or ac voltages of more than 300 mV between the two ground planes can not only damage ICs but cause false triggering of logic gates and possible latchup.

Grounding and Decoupling Mixed-Signal ICs with Low Digital Currents

Sensitive analog components such as amplifiers and voltage references are always referenced and decoupled to the analog ground plane. *The ADCs and DACs (and other mixed-signal ICs) with low digital currents should generally be treated as analog components and also grounded and decoupled to the analog ground plane*. At first glance, this may seem somewhat contradictory, since a converter has an analog and digital interface and usually has pins designated as *analog ground* (AGND) and *digital ground* (DGND). The diagram shown in Figure 9.26 will help to explain this seeming dilemma.

Inside an IC that has both analog and digital circuits, such as an ADC or a DAC, the grounds are usually kept separate to avoid coupling digital signals into the analog circuits. Figure 9.26 shows a simple model of a converter. There is nothing the IC designer can do about the wirebond inductance and resistance associated with connecting the bond pads on the chip to the package pins except to realize it's there. The rapidly changing digital currents produce a voltage at point B which will inevitably couple into point A of the analog circuits through the stray capacitance, C_{STRAY}. In addition, there is approximately 0.2-pF unavoidable stray capacitance between every pin of the IC package! It's the IC designer's job to make the chip work in spite of this. However, in order to prevent further coupling, the AGND and DGND pins should be joined together

externally to the *analog* ground plane with minimum lead lengths. Any extra impedance in the DGND connection will cause more digital noise to be developed at point B; it will, in turn, couple more digital noise into the analog circuit through the stray capacitance. *Note that connecting DGND to the digital ground plane applies V_{NOISE} across the AGND and DGND pins and invites disaster!*

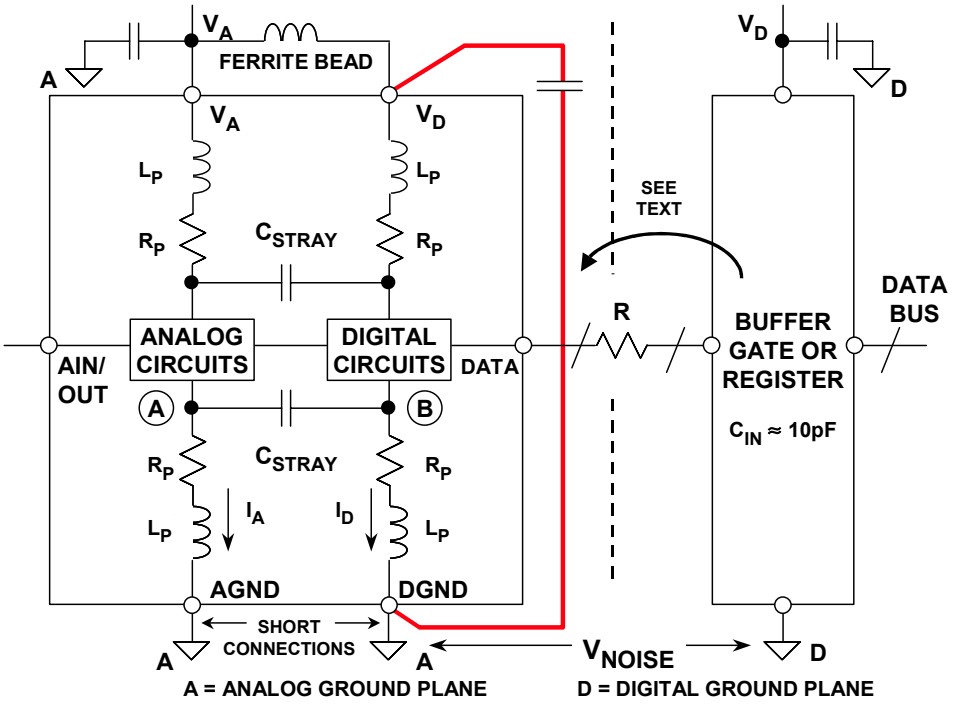


Figure 9.26: *Proper Grounding of Mixed-signal ICs With Low Internal Digital Currents*

The name "DGND" on an IC tells us that this pin connects to the digital ground of the IC. This does not imply that this pin must be connected to the digital ground of the system.

It is true that this arrangement may inject a small amount of digital noise onto the analog ground plane. These currents should be quite small, and can be minimized by ensuring that the converter output does not drive a large fanout (they normally can't, by design). Minimizing the fanout on the converter's digital port will also keep the converter logic transitions relatively free from ringing and minimize digital switching currents, and thereby reducing any potential coupling into the analog port of the converter. The logic supply pin (V_D) can be further isolated from the analog supply by the insertion of a small lossy ferrite bead as shown in Figure 9.26. The internal transient digital currents of the converter will flow in the small loop from V_D through the decoupling capacitor and to DGND (this path is shown with a heavy line on the diagram). The transient digital currents will therefore not appear on the external analog ground plane, but are confined to the loop. The V_D pin decoupling capacitor should be mounted as close to the converter as possible to minimize parasitic inductance. These decoupling capacitors should be low inductance ceramic types, typically between 0.01 µF and 0.1 µF.

Treat the ADC Digital Outputs with Care

It is always a good idea (as shown in Figure 9.26) to place a buffer register adjacent to the converter to isolate the converter's digital lines from noise on the data bus. The register also serves to minimize loading on the digital outputs of the converter and acts as a Faraday shield between the digital outputs and the data bus. Even though many converters have three-state outputs/inputs, this isolation register still represents good design practice. In some cases it may be desirable to add an additional buffer register on the analog ground plane next to the converter output to provide greater isolation.

The series resistors (labeled "R" in Figure 9.26) between the ADC output and the buffer register input help to minimize the digital transient currents which may affect converter performance. The resistors isolate the digital output drivers from the capacitance of the buffer register inputs. In addition, the RC network formed by the series resistor and the buffer register input capacitance acts as a lowpass filter to slow down the fast edges.

A typical CMOS gate combined with PCB trace and a through-hole will create a load of approximately 10 pF. A logic output slew rate of 1 V/ns will produce 10 mA of dynamic current if there is no isolation resistor:

$$\Delta I = C\frac{\Delta v}{\Delta t} = 10\ \text{pF} \times \frac{1\ \text{V}}{\text{ns}} = 10\ \text{mA}\,. \qquad \text{Eq. 9.2}$$

A 500Ω series resistors will minimize this output current and result in a rise and fall time of approximately 11ns when driving the 10pF input capacitance of the register:

$$t_r = 2.2 \times \tau = 2.2 \times R \cdot C = 2.2 \times 500\ \Omega \times 10\ \text{pF} = 11\ \text{ns}. \qquad \text{Eq. 9.3}$$

TTL registers should be avoided, since they can appreciably add to the dynamic switching currents because of their higher input capacitance.

The buffer register and other digital circuits should be grounded and decoupled to the *digital* ground plane of the PC board. Notice that any noise between the analog and digital ground plane reduces the noise margin at the converter digital interface. Since digital noise immunity is of the orders of hundreds or thousands of millivolts, this is unlikely to matter. The analog ground plane will generally not be very noisy, but if the noise on the digital ground plane (relative to the analog ground plane) exceeds a few hundred millivolts, then steps should be taken to reduce the digital ground plane impedance, thereby maintaining the digital noise margins at an acceptable level. Under no circumstances should the voltage between the two ground planes exceed 300 mV, or the ICs may be damaged.

Separate power supplies for analog and digital circuits are also highly desirable, even if the voltages are the same. The analog supply should be used to power the converter. If the converter has a pin designated as a digital supply pin (V_D), it should either be powered from a separate analog supply, or filtered as shown in the diagram. All converter power pins should be decoupled to the analog ground plane, and all logic circuit power pins should be decoupled to the digital ground plane as shown in Figure 9.27.

In some cases it may not be possible to connect V_D to the analog supply. Some of the newer, high speed ICs may have their analog circuits powered by +5 V, but the digital interface powered by +3 V to interface to 3-V logic. In this case, the +3-V pin of the IC should be decoupled directly to the analog ground plane. It is also advisable to connect a ferrite bead in series with the power trace that connects the pin to the +3-V digital logic supply.

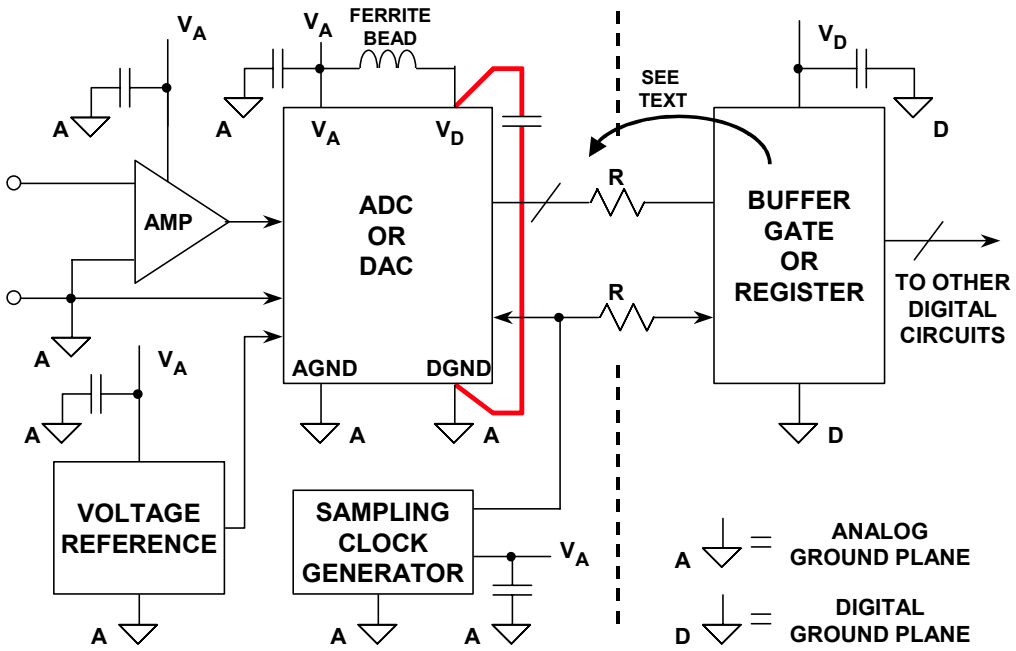


Figure 9.27: *Grounding and Decoupling Points*

The sampling clock generation circuitry should be treated like analog circuitry and also be grounded and heavily-decoupled to the analog ground plane. Phase noise on the sampling clock produces degradation in system SNR as will be discussed shortly.

Sampling Clock Considerations

In a high performance sampled data system a low phase-noise crystal oscillator should be used to generate the ADC (or DAC) sampling clock because sampling clock jitter modulates the analog input/output signal and raises the noise and distortion floor. The sampling clock generator should be isolated from noisy digital circuits and grounded and decoupled to the analog ground plane, as is true for the op amp and the ADC.

The effect of sampling clock jitter on ADC signal-to-soise ratio (SNR) is given approximately by the equation:

$$\mathrm{SNR} = 20\log_{10}\left[\frac{1}{2\pi f t_j}\right], \qquad \text{Eq. 9.4}$$

where SNR is the SNR of a perfect ADC of infinite resolution where the only source of noise is that caused by the rms sampling clock jitter, t_j. Note that f in the above equation is the analog input frequency. Just working through a simple example, if t_j = 50 ps rms, f = 100 kHz, then SNR = 90 dB, equivalent to about 15-bit dynamic range.

It should be noted that t_j in the above example is the root-sum-square (rss) value of the external clock jitter *and* the internal ADC clock jitter (called aperture jitter). However, in most high performance ADCs, the internal aperture jitter is negligible compared to the jitter on the sampling clock.

Since degradation in SNR is primarily due to external clock jitter, steps must be taken to ensure the sampling clock is as noise-free as possible and has the lowest possible phase jitter. This requires that a crystal oscillator be used. There are several manufacturers of small crystal oscillators with low jitter (less than 5-ps rms) CMOS compatible outputs. (For example, MF Electronics, 10 Commerce Dr., New Rochelle, NY 10801, Tel. 914-576-6570 and Wenzel Associates, Inc., 2215 Kramer Lane, Austin, Texas 78758 Tel. 512- 835-2038).

Ideally, the sampling clock crystal oscillator should be referenced to the analog ground plane in a split-ground system. However, this is not always possible because of system constraints. In many cases, the sampling clock must be derived from a higher frequency multi-purpose system clock which is generated on the digital ground plane. It must then pass from its origin on the digital ground plane to the ADC on the analog ground plane. Ground noise between the two planes adds directly to the clock signal and will produce excess jitter. The jitter can cause degradation in the signal-to-noise ratio and also produce unwanted harmonics.

This can be remedied somewhat by transmitting the sampling clock signal as a differential signal using either a small RF transformer as shown in Figure 9.28 or a high speed differential driver and receiver IC. If an active differential driver and receiver are used, they should be ECL to minimize phase jitter. In a single +5-V supply system, ECL logic can be connected between ground and +5 V (PECL), and the outputs ac coupled into the ADC sampling clock input. In either case, the original master system clock must be generated from a low phase noise crystal oscillator, and not the clock output of a DSP, microprocessor, or microcontroller.

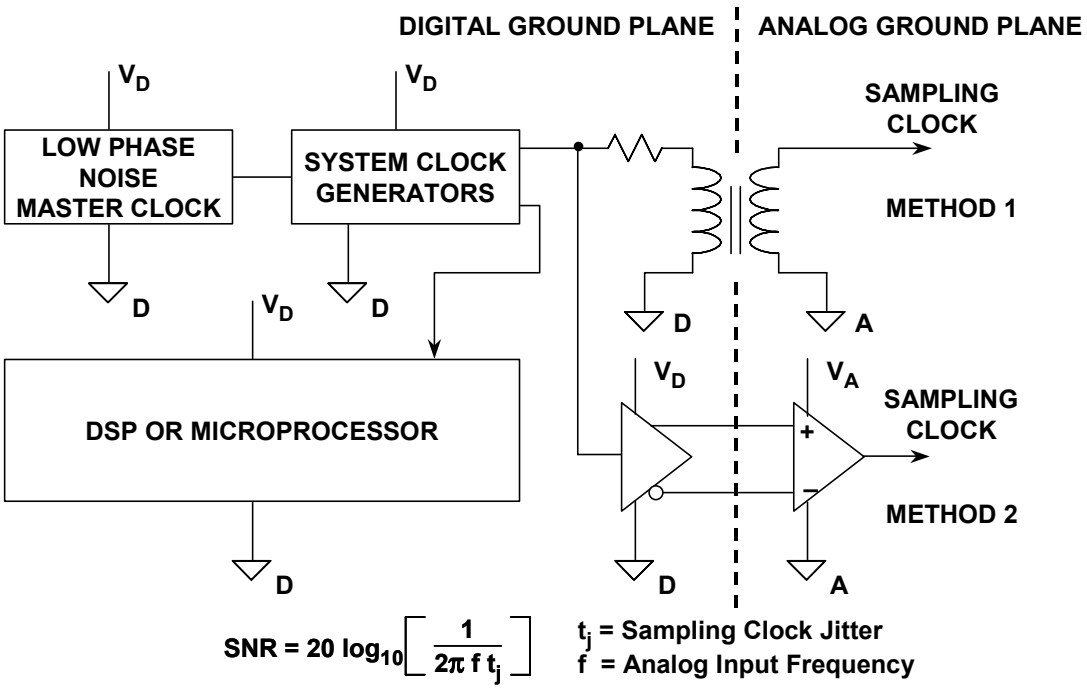


Figure 9.28: *Sampling Clock Distribution From Digital to Analog Ground Planes*

The Origins of the Confusion about Mixed-Signal Grounding: Applying Single-Card Grounding Concepts to Multicard Systems

Most ADC, DAC, and other mixed-signal device data sheets discuss grounding relative to a single PCB, usually the manufacturer's own evaluation board. This has been a source of confusion when trying to apply these principles to multicard or multi-ADC/DAC systems. The recommendation is usually to split the PCB ground plane into an analog plane and a digital plane. It is then further recommended that the AGND and DGND pins of a converter be tied together and that the analog ground plane and digital ground planes be connected at that same point as shown in Figure 9.29. This essentially creates the system "star" ground at the mixed-signal device.

All noisy digital currents flow through the digital power supply to the digital ground plane and back to the digital supply; they are isolated from the sensitive analog portion of the board. The system star ground occurs where the analog and digital ground planes are joined together at the mixed signal device. While this approach will generally work in a simple system with a single PCB and single ADC/DAC, it is not optimum for multicard mixed-signal systems. In systems having several ADCs or DACs on different PCBs (or on the same PCB, for that matter), the analog and digital ground planes become connected at several points, creating the possibility of ground loops and making a single-point "star" ground system impossible. For these reasons, this grounding approach is not recommended for multicard systems, and the approach previously discussed should be used for mixed signal ICs with low digital currents.

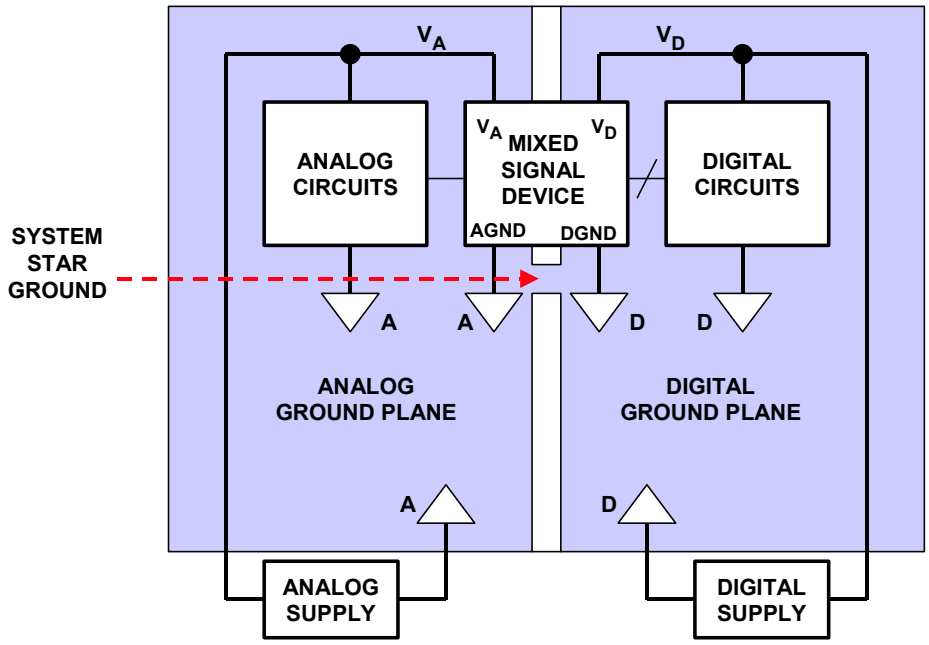


Figure 9.29: *Grounding Mixed Signal ICs : Single PC Board (Typical Evaluation/Test Board)*

Summary: Grounding Mixed Signal Devices with Low Digital Currents in a Multicard System

Figure 9.30 summarizes the approach previously described for grounding a mixed signal device which has low digital currents. The analog ground plane is not corrupted because the small digital transient currents flow in the small loop between V_D, the decoupling capacitor, and DGND (shown as a heavy line). The mixed signal device is for all intents and purposes treated as an analog component. The noise V_N between the ground planes reduces the noise margin at the digital interface but is generally not harmful if kept less than 300 mV by using a low impedance digital ground plane all the way back to the system star ground.

However, mixed signal devices such as sigma-delta ADCs, codecs, and DSPs with on-chip analog functions are becoming more and more digitally intensive. Along with the additional digital circuitry come larger digital currents and noise. For example, a sigma-delta ADC or DAC contains a complex digital filter which adds considerably to the digital current in the device. The method previously discussed depends on the decoupling capacitor between V_D and DGND to keep the digital transient currents isolated in a small loop. However, if the digital currents are significant enough and have components at dc or low frequencies, the decoupling capacitor may have to be so large that it is impractical. Any digital current which flows outside the loop between V_D and DGND must flow through the analog ground plane. This may degrade performance, especially in high resolution systems.

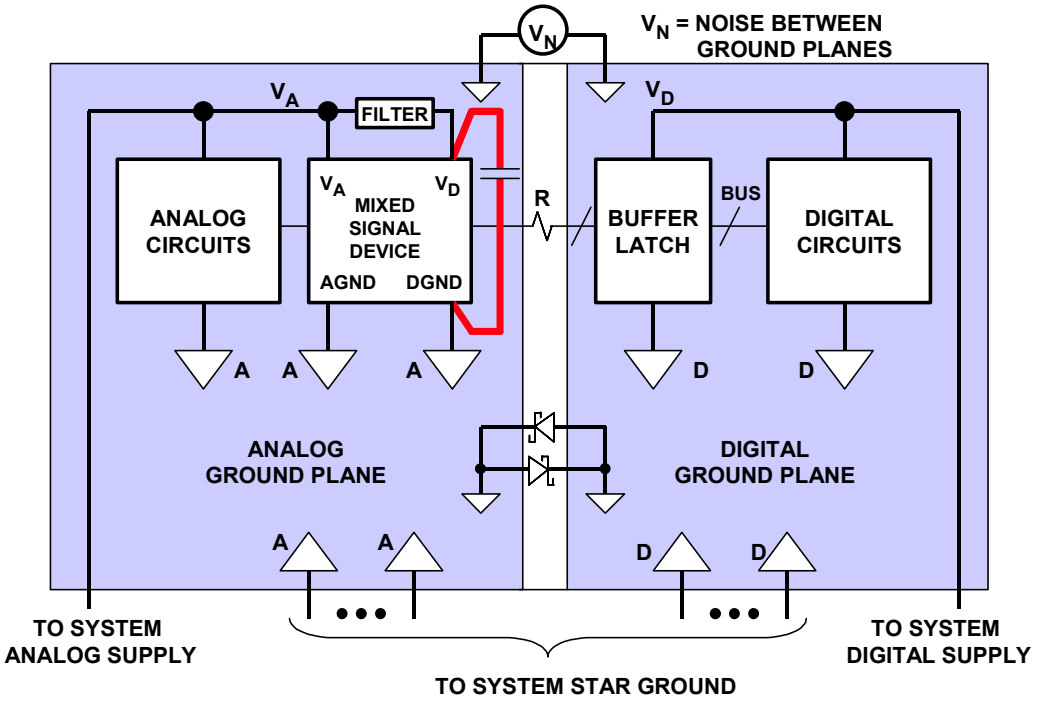


Figure 9.30: *Grounding Mixed Signal ICs with Low Internal Digital Currents: Multiple PC Boards*

It is difficult to predict what level of digital current flowing into the analog ground plane will become unacceptable in a system. All we can do at this point is to suggest an alternative grounding method which may yield better performance.

Summary: Grounding Mixed Signal Devices with High Digital Currents in a Multicard System

An alternative grounding method for a mixed signal device with high levels of digital currents is shown in Figure 9.31. The AGND of the mixed signal device is connected to the analog ground plane, and the DGND of the device is connected to the digital ground plane. The digital currents are isolated from the analog ground plane, but the noise between the two ground planes is applied directly between the AGND and DGND pins of the device. For this method to be successful, the analog and digital circuits within the mixed signal device must be well isolated. The noise between AGND and DGND pins must not be large enough to reduce internal noise margins or cause corruption of the internal analog circuits.

Figure 9.31 shows optional Schottky diodes (back-to-back) or a ferrite bead connecting the analog and digital ground planes. The Schottky diodes prevent large dc voltages or low frequency voltage spikes from developing across the two planes. These voltages can potentially damage the mixed signal IC if they exceed 300 mV because they appear directly between the AGND and DGND pins. As an alternative to the back-to-back Schottky diodes, a ferrite bead provides a dc connection between the two planes but isolates them at frequencies above a few MHz where the ferrite bead becomes resistive. This protects the IC from dc voltages between AGND and DGND, but the dc connection

provided by the ferrite bead can introduce unwanted dc ground loops and may not be suitable for high resolution systems.

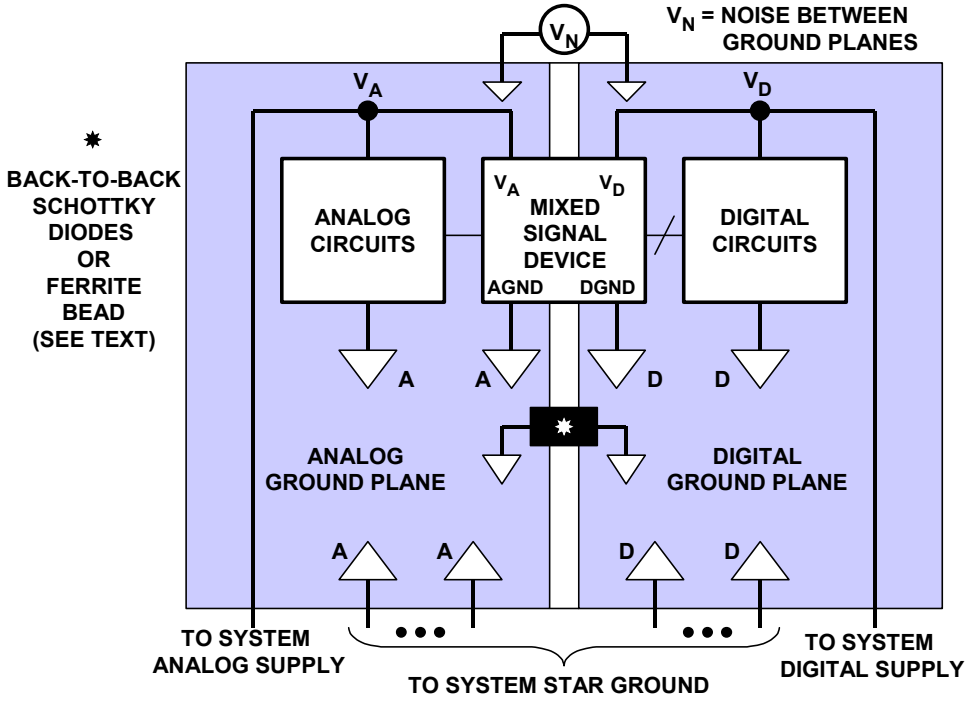


Figure 9.31: *Grounding Alternative for Mixed-Signal ICs with High Digital Currents: Multiple PC Boards*

Grounding DSPs with Internal Phase-Locked Loops

As if dealing with mixed-signal ICs with AGND and DGNDs wasn't enough, DSPs such as the ADSP-21160 SHARC with internal phase-locked-loops (PLLs) raise issues with respect to proper grounding. The ADSP-21160 PLL allows the internal core clock (determines the instruction cycle time) to operate at a user-selectable ratio of 2, 3, or 4 times the external clock frequency, CLKIN. The CLKIN rate is the rate at which the synchronous external ports operate. Although this allows using a lower frequency external clock, care must be taken with the power and ground connections to the internal PLL as shown in Figure 9.32.

In order to prevent internal coupling between digital currents and the PLL, the power and ground connections to the PLL are brought out separately on pins labeled AV_{DD} and AGND, respectively. The AV_{DD} +2.5-V supply should be derived from the $V_{DD\ INT}$ +2.5-V supply using the filter network as shown. This ensures a relatively noise-free supply for the internal PLL. The AGND pin of the PLL should be connected to the digital ground plane of the PC board using a short trace. The decoupling capacitors should be routed between the AV_{DD} pin and AGND pin using short traces.

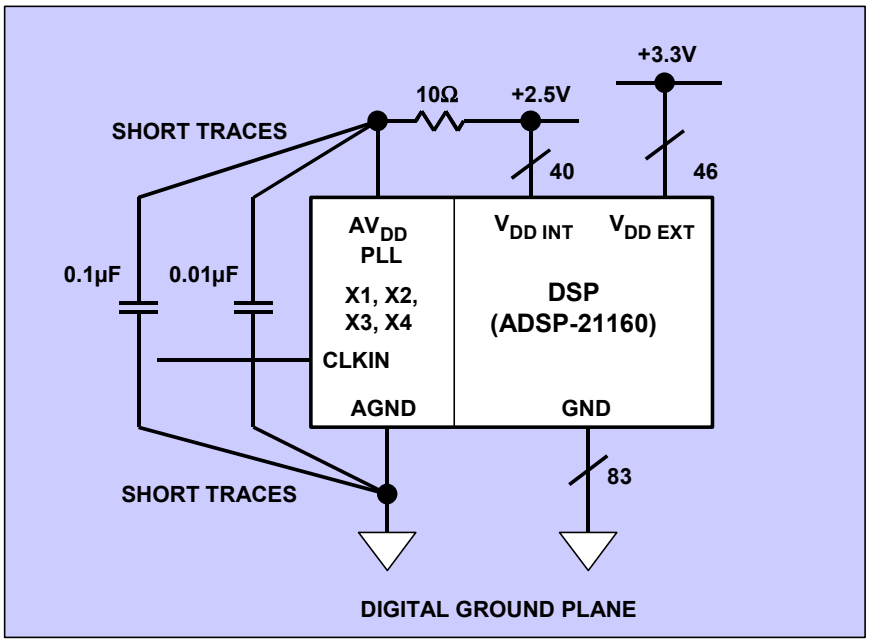


Figure 9.32: *Grounding DSPs with Internal Phase-Locked-Loops (PLLs)*

Grounding Summary

There is no single grounding method which will guarantee optimum performance 100% of the time! This section has presented a number of possible options depending upon the characteristics of the particular mixed signal devices in question. It is helpful, however, to provide for as many options as possible when laying out the initial PC board.

It is mandatory that at least one layer of the PC board be dedicated to ground plane! The initial board layout should provide for non-overlapping analog and digital ground planes, but pads and vias should be provided at several locations for the installation of back-to-back Schottky diodes or ferrite beads, if required. Pads and vias should also be provided so that the analog and digital ground planes can be connected together with jumpers if required.

The AGND pins of mixed-signal devices should in general always be connected to the analog ground plane. An exception to this are DSPs which have internal phase-locked-loops (PLLs), such as the ADSP-21160 SHARC. The ground pin for the PLL is labeled AGND, but should be connected directly to the digital ground plane for the DSP. See Figure 9.33 for a general summary of grounding philosophy.

- **There is no single grounding method which is guaranteed to work 100% of the time!**
- **Different methods may or may not give the same levels of performance.**
- **At least one layer on each PC board MUST be dedicated to ground plane!**
- **Do initial layout with split analog and digital ground planes.**
- **Provide pads and vias on each PC board for back-to-back Schottky diodes and optional ferrite beads to connect the two planes.**
- **Provide "jumpers" so that DGND pins of mixed-signal devices can be connected to AGND pins (analog ground plane) or to digital ground plane. (AGND of PLLs in DSPs should be connected to digital ground plane).**
- **Provide pads and vias for "jumpers" so that analog and digital ground planes can be joined together at several points on each PC board.**
- **Follow recommendations on mixed signal device data sheet.**

Figure 9.33: *Grounding Philosophy Summary*

Some General PC Board Layout Guidelines for Mixed-Signal Systems

It is evident that noise can be minimized by paying attention to the system layout and preventing different signals from interfering with each other. High level analog signals should be separated from low level analog signals, and both should be kept away from digital signals. We have seen elsewhere that in waveform sampling and reconstruction systems the sampling clock (which is a digital signal) is as vulnerable to noise as any analog signal, but is as liable to cause noise as any digital signal, and so must be kept isolated from both analog and digital systems. If clock driver packages are used in clock distribution, only one frequency clock should be passed through a single package. Sharing drivers between clocks of different frequencies in the same package will produce excess jitter and crosstalk and degrade performance.

The ground plane can act as a shield where sensitive signals cross. Figure 9.34 shows a good layout for a data acquisition board where all sensitive areas are isolated from each other and signal paths are kept as short as possible. While real life is rarely as tidy as this, the principle remains a valid one.

There are a number of important points to be considered when making signal and power connections. First of all a connector is one of the few places in the system where all signal conductors must run in parallel—it is therefore imperative to separate them with ground pins (creating a faraday shield) to reduce coupling between them.

Multiple ground pins are important for another reason: they keep down the ground impedance at the junction between the board and the backplane. The contact resistance of a single pin of a PCB connector is quite low (of the order of 10 mΩ) when the board is new—as the board gets older the contact resistance is likely to rise, and the board's performance may be compromised. It is therefore well worthwhile to allocate extra PCB connector pins so that there are many ground connections (perhaps 30-40% of all the pins

on the PCB connector should be ground pins). For similar reasons there should be several pins for each power connection, although there is no need to have as many as there are ground pins.

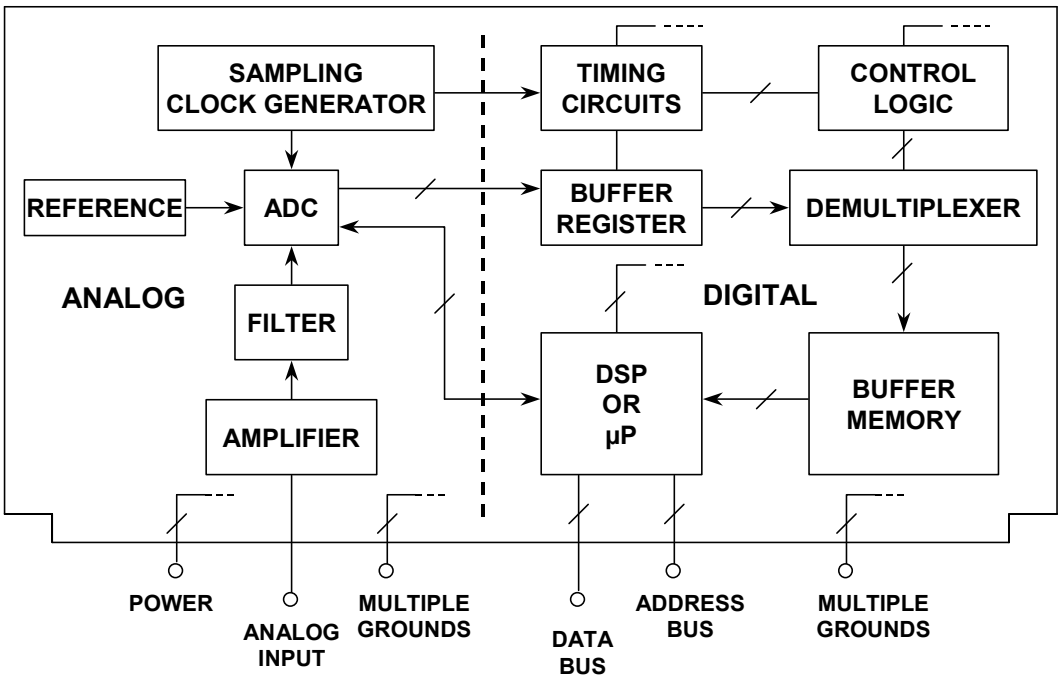


Figure 9.34: *Analog and Digital Circuits Should be Partitioned on PCB Layout*

Analog Devices and other manufacturers of high performance mixed-signal ICs offer evaluation boards to assist customers in their initial evaluations and layout. ADC evaluation boards generally contain an on-board low-jitter sampling clock oscillator, output registers, and appropriate power and signal connectors. They also may have additional support circuitry such as the ADC input buffer amplifier and external reference.

The layout of the evaluation board is optimized in terms of grounding, decoupling, and signal routing and can be used as a model when laying out the ADC PC board in the system. The actual evaluation board layout is usually available from the ADC manufacturer in the form of computer CAD files (Gerber files). In many cases, the layout of the various layers appears on the data sheet for the device.

Skin Effect

At high frequencies, also consider *skin effect*, where inductive effects cause currents to flow only in the outer surface of conductors. Note that this is in contrast to the earlier discussions of this section on dc resistance of conductors.

The skin effect has the consequence of increasing the resistance of a conductor at high frequencies. Note also that this effect is separate from the increase in impedance due to the effects of the self-inductance of conductors as frequency is increased.

Skin effect is quite a complex phenomenon, and detailed calculations are beyond the scope of this discussion. However, a good approximation for copper is that the skin depth in centimeters is $6.61/\sqrt{f}$, (f in Hz).

A summary of the skin effect within a typical PCB conductor foil is shown in Figure 9.35. Note that this copper conductor cross-sectional view assumes looking into the *side* of the conducting trace.

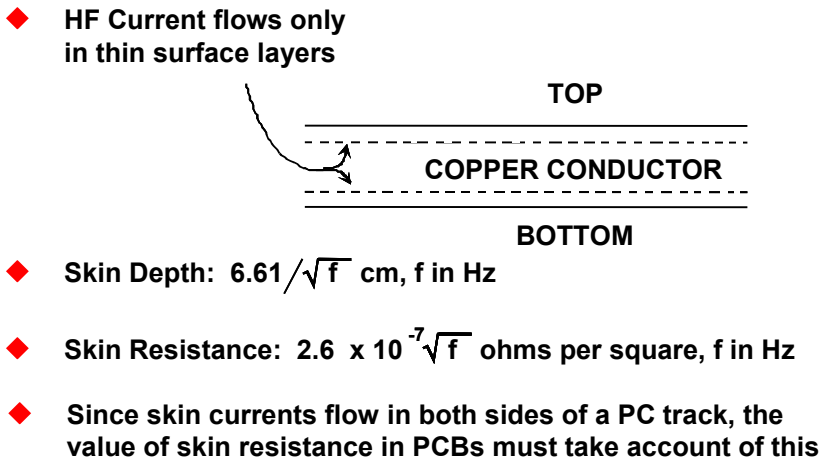


Figure 9.35: *Skin Depth in a PC Conductor*

Assuming that skin effects become important when the skin depth is less than 50% of the thickness of the conductor, this tells us that for a typical PC foil, we must be concerned about skin effects at frequencies above approximately 12 MHz.

Where skin effect is important, the resistance for copper is $2.6 \times 10^{-7} \sqrt{f}$ ohms per square, (f in Hz). This formula is invalid if the skin thickness is greater than the conductor thickness (i.e. at dc or low frequencies).

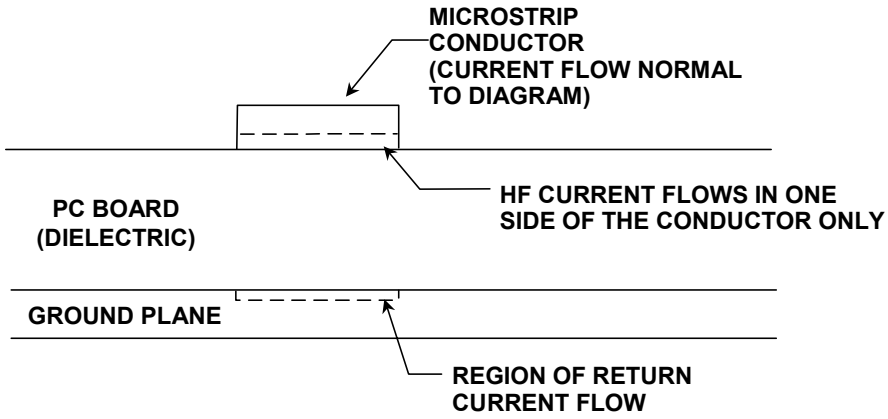


Figure 9.36: *Skin Effect with PC Conductor and Ground Plane*

Figure 9.36 illustrates a case of a PCB conductor with current flow, as separated from the ground plane underneath.

In this diagram, note the (dotted) regions of high frequency current flow, as reduced by the skin effect. When calculating skin effect in PCBs, it is important to remember that current generally flows in both sides of the PC foil (this is not necessarily the case in microstrip lines, see below), so the resistance per square of PC foil may be half the above value.

Transmission Lines

We earlier considered the benefits of outward and return signal paths being close together so that inductance is minimized. As shown previously in Figure 9.36, when a high frequency signal flows in a PC track running over a ground plane, the arrangement functions as a *microstrip* transmission line, and the majority of the return current flows in the ground plane underneath the line.

Figure 9.37 shows the general parameters for a microstrip transmission line, given the conductor width, w, dielectric thickness, h, and the dielectric constant, E_r.

The characteristic impedance of such a microstrip line will depend upon the width of the track and the thickness and dielectric constant of the PCB material. Designs of microstrip lines are covered in more detail later in this chapter.

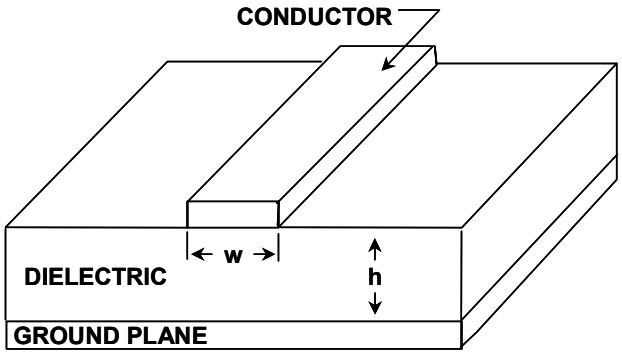


Figure 9.37: *A PCB Microstrip Transmission Line is an Example of a Controlled Impedance Conductor Pair*

For most dc and lower frequency applications, the characteristic impedance of PCB traces will be relatively unimportant. Even at frequencies where a track over a ground plane behaves as a transmission line, it is not necessary to worry about its characteristic impedance or proper termination if the free space wavelengths of the frequencies of interest are greater than ten times the length of the line.

However, at VHF and higher frequencies it is possible to use PCB tracks as microstrip lines within properly terminated transmission systems. Typically the microstrip will be designed to match standard coaxial cable impedances, such as 50, 75 or 100 Ω, simplifying interfacing.

Note that if losses in such systems are to be minimized, the PCB material must be chosen for low high-frequency losses. This usually means the use of Teflon or some other comparably low-loss PCB material. Often, though, the losses in short lines on cheap glass-fiber board are small enough to be quite acceptable.

Be Careful With Ground Plane Breaks

Wherever there is a break in the ground plane beneath a conductor, the ground plane return current must by necessity flow *around* the break. As a result, both the inductance and the vulnerability of the circuit to external fields are increased. This situation is diagrammed in Figure 9.38, where conductors A and B must cross one another.

Where such a break is made to allow a crossover of two perpendicular conductors, it would be far better if the second signal were carried across both the first and the ground plane by means of a piece of wire or a resistor. The ground plane then acts as a shield between the two signal conductors, and the two ground return currents, flowing in opposite sides of the ground plane as a result of skin effects, do not interact.

With a multi-layer board, both the crossover and the continuous ground plane can be accommodated without the need for a wire link. Multi-layer PCBs are expensive and harder to trouble-shoot than more simple double-sided boards, but do offer even better shielding and signal routing. The principles involved remain unchanged but the range of layout options is increased.

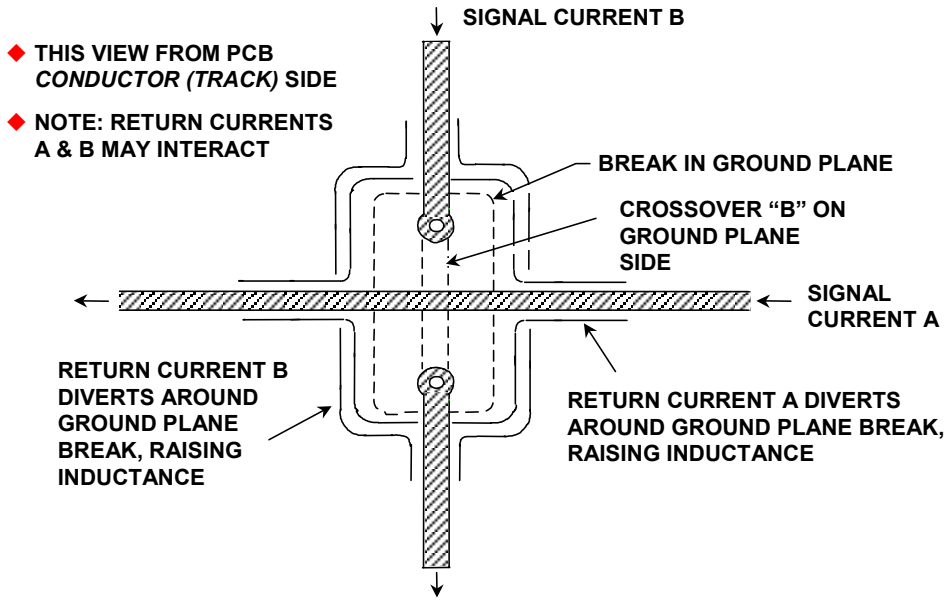


Figure 9.38: *A Ground Plane Break Raises Circuit Inductance, and Increases Vulnerability to External Fields*

The use of double-sided or multi-layer PCBs with at least one continuous ground plane is undoubtedly one of the most successful design approaches for high performance mixed signal circuitry. Often the impedance of such a ground plane is sufficiently low to permit the use of a single ground plane for both analog and digital parts of the system. However, whether or not this is possible does depend upon the resolution and bandwidth required, and the amount of digital noise present in the system.

Ground Isolation Techniques

While the use of ground planes does lower impedance and helps greatly in lowering ground noise, there may still be situations where a prohibitive level of noise exists. In such cases, the use of ground error minimization and isolation techniques can be helpful.

Another illustration of a common-ground impedance coupling problem is shown in Figure 9.39. In this circuit a precision gain-of-100 preamp amplifies a low-level signal V_{IN}, using an AD8551 chopper-stabilized amplifier for best dc accuracy. At the load end, the signal V_{OUT} is measured with respect to G2, the local ground. Because of the small 700-µA I_{SUPPLY} of the AD8551 flowing between G1 and G2, there is a 7-µV ground error—about 7 times the typical input offset expected from the op amp!

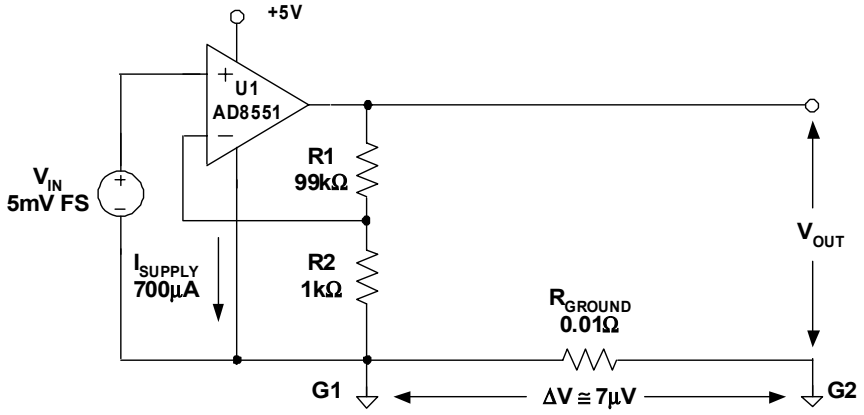


Figure 9.39: *Unless Care is Taken, Even Small Common Ground Currents can Degrade Precision Amplifier Accuracy*

This error can be avoided by routing the negative supply pin current of the op amp back to star ground G2 as opposed to ground G1, by using a separate trace. This step eliminates the G1-G2 path power supply current, and so minimizes the ground leg voltage error. Note that there will be little error developed in the "hot" V_{OUT} lead, so long as the current drain at the load end is small.

In some cases, there may be simply unavoidable ground voltage differences between a source signal and the load point where it is to be measured. Within the context of this "same-board" discussion, this might require rejecting ground error voltages of several tens-of-mV. Or, should the source signal originate from an "off-board" source, then the magnitude of the common-mode voltages to be rejected can easily rise into a several volt range (or even tens-of-volts).

Fortunately, full signal transmission accuracy can still be accomplished in the face of such high noise voltages, by employing a principle discussed earlier. This is the use of a differential-input, *ground isolation* amplifier. The ground isolation amplifier minimizes the effect of ground error voltages between stages by processing the signal in differential fashion, thereby rejecting common-mode voltages by a substantial margin (typically 60 dB or more). Note that this approach is only effective for very low frequency signals, however.

Two ground isolation amplifier solutions are shown in Figure 9.40. This diagram can alternately employ either the AD629 to handle CM voltages up to ±270 V, or the AMP03, which is suitable for CM voltages up to ±20 V.

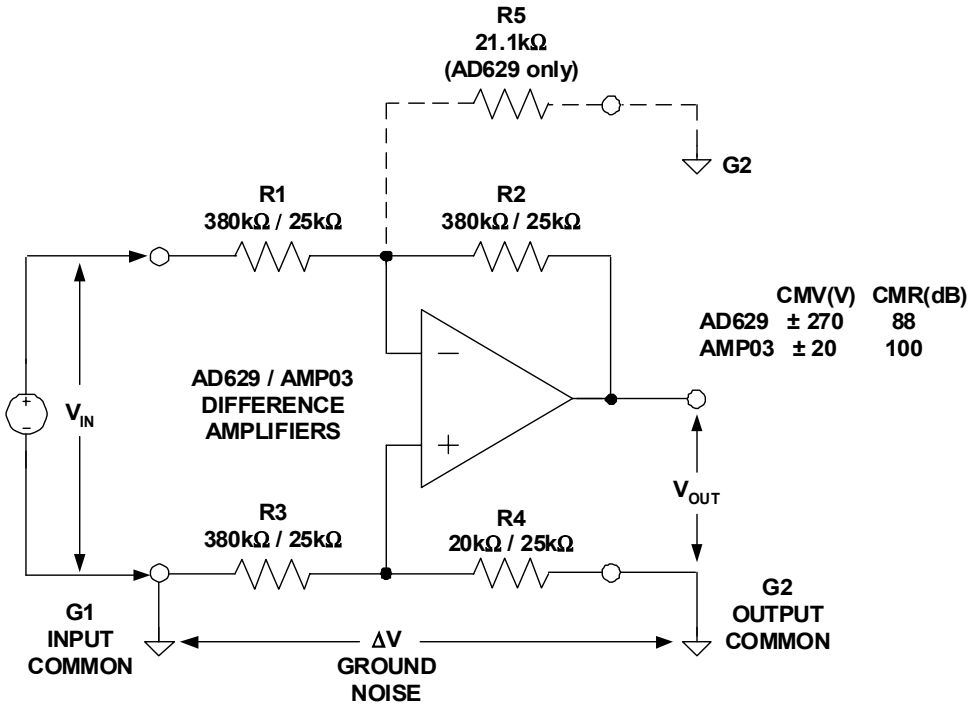


Figure 9.40: *A Differential Input Ground Isolating Amplifier Allows High Transmission Accuracy by Rejecting Ground Noise Voltage Between Source (G1) and Measurement (G2) Grounds*

In the circuit, input voltage V_{IN} is referred to G1, but must be measured with respect to G2. With the use of a high CMR unity-gain difference amplifier, the noise voltage ΔV existing between these two grounds is easily rejected. The AD629 offers a typical CMR of 88 dB, while the AMP03 typically achieves 100 dB. In the AD629, the high CMV rating is done by a combination of high CM attenuation, followed by differential gain, realizing a net differential gain of unity. The AD629 uses the first listed value resistors noted in the figure for R1-R5. The AMP03 operates as a precision four-resistor differential amplifier, using the 25-kΩ value R1-R4 resistors noted. Both devices are complete, one package solutions to the ground-isolation amplifier.

This scheme allows relative freedom from tightly controlling ground drop voltages, or running additional and/or larger PCB traces to minimize such error voltages. Note that it can be implemented either with the fixed gain difference amplifiers shown, or also with a

standard in-amp IC, configured for unity gain. The AD623, for example, also allows single-supply use. In any case, signal polarity is also controllable, by simple reversal of the difference amplifier inputs.

In general terms, transmitting a signal from one point on a PCB to another for measurement or further processing can be optimized by two key interrelated techniques. These are the use of high-impedance, differential signal-handling techniques. The high impedance loading of an in-amp minimizes voltage drops, and differential sensing of the remote voltage minimizes sensitivity to ground noise.

When the further signal processing is A/D conversion, these transmission criteria can be implemented *without* adding a differential ground isolation amplifier stage. Simply select an ADC which operates differentially. The high input impedance of the ADC minimizes load sensitivity to the PCB wiring resistance. In addition, the differential input feature allows the output of the source to be sensed directly at the source output terminals (even if single-ended). The CMR of the ADC then eliminates sensitivity to noise voltages between the ADC and source grounds.

An illustration of this concept using an ADC with high impedance differential inputs is shown in Figure 9.41. Note that the general concept can be extended to virtually any signal source, driving any load. All loads, even single-ended ones, become differential-input by adding an appropriate differential input stage.

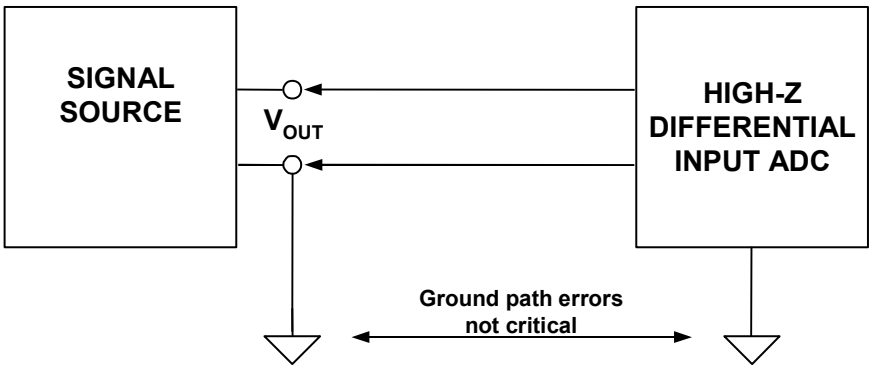


Figure 9.41: *A High-Impedance Differential Input ADC Also Allows High Transmission Accuracy Between Source and Load*

The differential input can be provided by either a fully developed high-Z in-amp, or in many cases it can be a simple subtractor stage op amp, such as Figure 9.40.

Static PCB Effects

Leakage resistance is the dominant static circuit board effect. Contamination of the PCB surface by flux residues, deposited salts, and other debris can create leakage paths between circuit nodes. Even on well-cleaned boards, it is not unusual to find 10 nA or more of leakage to nearby nodes from 15-V supply rails. Nanoamperes of leakage current into the wrong nodes often cause volts of error at a circuit's output; for example, 10 nA into a 10-MΩ resistance causes a 0.1-V error. Unfortunately, the standard op amp pinout

places the $-V_S$ supply pin next to the + input, which is often hoped to be at high impedance! To help identify nodes sensitive to the effects of leakage currents ask the simple question: If a spurious current of a few nanoamperes or more were injected into this node, would it matter?

If the circuit is already built, you can localize moisture sensitivity to a suspect node with a classic test. While observing circuit operation, blow on potential trouble spots through a simple soda straw. The straw focuses the breath's moisture, which, with the board's salt content in susceptible portions of the design, disrupts circuit operation upon contact. There are several means of eliminating simple surface leakage problems. Thorough washing of circuit boards to remove residues helps considerably. A simple procedure includes vigorously brushing the boards with isopropyl alcohol, followed by thorough washing with deionized water and an 85°C bakeout for a few hours. Be careful when selecting board-washing solvents, though. When cleaned with certain solvents, some water-soluble fluxes create salt deposits, exacerbating the leakage problem.

Unfortunately, if a circuit displays sensitivity to leakage, even the most rigorous cleaning can offer only a temporary solution. Problems soon return upon handling, or exposure to foul atmospheres, and high humidity. Some additional means must be sought to stabilize circuit behavior, such as conformal surface coating.

Fortunately, there is an answer to this, namely *guarding*, which offers a fairly reliable and permanent solution to the problem of surface leakage. Well-designed guards can eliminate leakage problems, even for circuits exposed to harsh industrial environments. Two schematics illustrate the basic guarding principle, as applied to typical inverting and non-inverting op amp circuits.

Figure 9.42 illustrates an inverting mode guard application. In this case, the op amp reference input is grounded, so the guard is a grounded ring surrounding all leads to the inverting input, as noted by the dotted line.

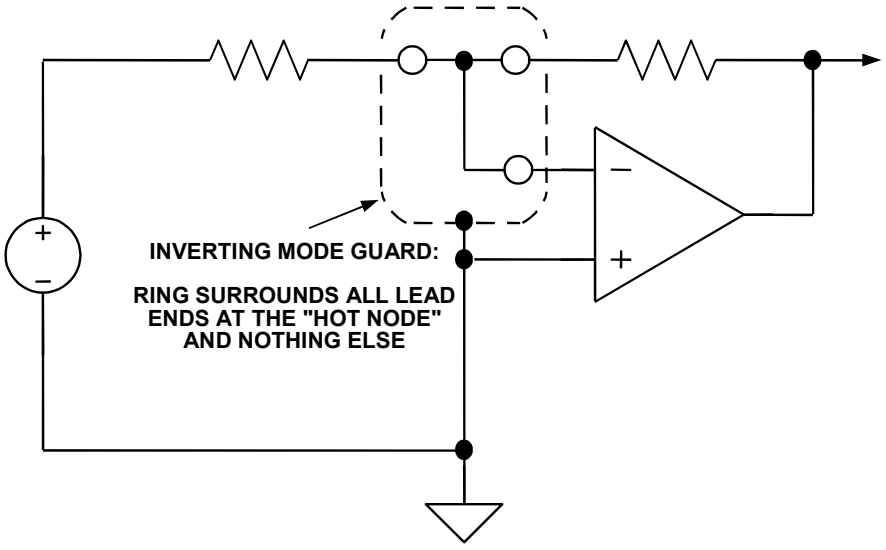


Figure 9.42: *Inverting Mode Guard Encloses All Op Amp Inverting Input Connections Within a Grounded Guard Ring*

Basic guarding principles are simple: *Completely* surround sensitive nodes with conductors that can readily sink stray currents, and maintain the guard conductors at the exact potential of the sensitive node (as otherwise the guard will serve as a leakage source rather than a leakage sink). For example, to keep leakage into a node below 1 pA (assuming 1000-MΩ leakage resistance) the guard and guarded node must be within 1 mV. Generally, the low offset of a modern op amp is sufficient to meet this criterion.

There are important caveats to be noted with implementing a true high-quality guard. For traditional through-hole PCB connections, the guard pattern should appear on *both* sides of the circuit board, to be most effective. And, it should also be connected along its length by several vias. Finally, when either justified or required by the system design parameters, do make an effort to include guards in the PCB design process from the outset—there is little likelihood that a proper guard can be added as an afterthought.

Figure 9.43 illustrates the case for a non-inverting guard. In this instance the op amp reference input is directly driven by the source, which complicates matters considerably. Again, the guard ring completely surrounds all of the input nodal connections. In this instance however, the guard is driven from the low impedance feedback divider connected to the inverting input.

Usually the guard-to-divider junction will be a direct connection, but in some cases a unity gain buffer might be used at "X" to drive a cable shield, or also to maintain the lowest possible impedance at the guard ring.

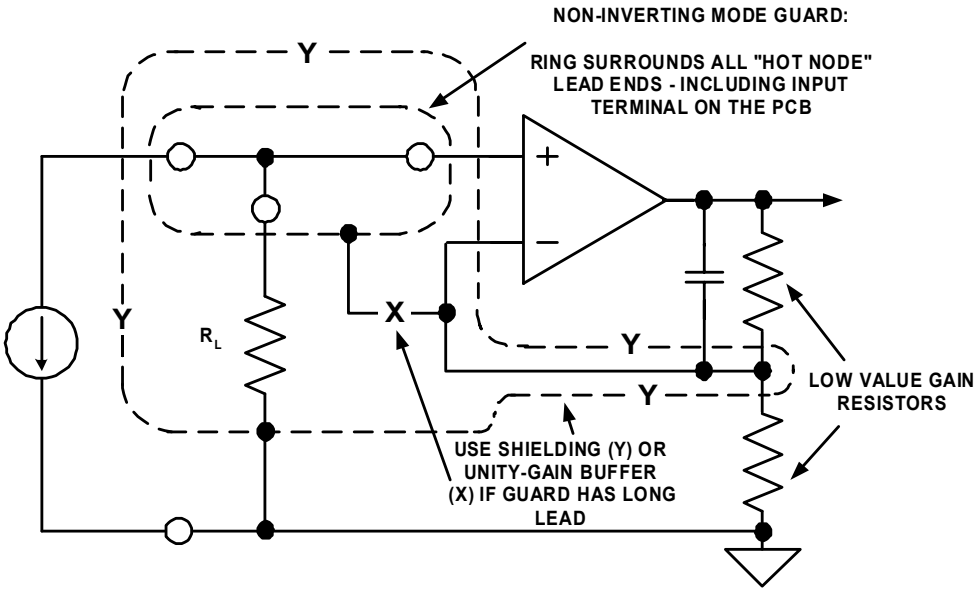


Figure 9.43: *Non-Inverting Mode Guard Encloses All Op Amp Non-Inverting Input Connections Within a Low Impedance, Driven Guard Ring*

In lieu of the buffer, another useful step is to use an additional, directly grounded screen ring, "Y", which surrounds the inner guard and the feedback nodes as shown. This step

costs nothing except some added layout time, and will greatly help buffer leakage effects into the higher impedance inner guard ring.

Of course what hasn't been addressed to this point is just how the op amp itself gets connected into these guarded islands without compromising performance. The traditional method using a TO-99 metal can package device was to employ double-sided PCB guard rings, with both op amp inputs terminated within the guarded ring.

Many high impedance sensors use the above-described method. The section immediately following illustrates how more modern IC packages can be mounted to PCB patterns, and take advantage of guarding and low-leakage operation.

Sample MINIDIP and SOIC Op Amp PCB Guard Layouts

Modern assembly practices have favored smaller plastic packages such as 8-pin MINIDIP and SOIC types. Some suggested partial layouts for guard circuits using these packages is shown in the next two figures. While guard traces may also be possible with even more tiny op amp footprints, such as SOT23, SC70, etc., the required trace separations become even more confining, challenging the layout designer as well as the manufacturing processes.

For the ADI "N" style MINIDIP package, Figure 9.44 illustrates how guarding can be accomplished for inverting (left) and non-inverting (right) operating modes. This setup would also be applicable to other op amp devices where relatively high voltages occur at pin 1 or 4. Using a standard 8-pin DIP outline for a single op amp, it can be noted that this package's 0.1" pin spacing allows a PC trace (here, the guard trace) to pass between adjacent pins. This is the key to implementing effective DIP package guarding, as it can adequately prevent a leakage path from the $-V_S$ supply at pin 4, or from similar high potentials at pin 1.

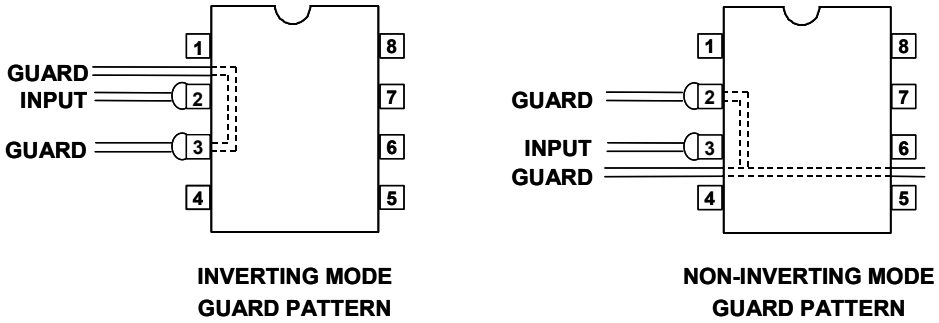


Figure 9.44: *PCB Guard Patterns for Inverting and Non-Inverting Mode Op Amps Using 8 Pin MINIDIP (N) Package*

For the left-side inverting mode, note that the grounded guard traces connected to pin 3 surround the op amp inverting input (pin 2), and run parallel to the input trace. This guard would be continued out to and around the source and feedback connections of Figure 9.42 (or other similar circuit), including an input pad in the case of a cable. In the

right-side non-inverting mode, the guard voltage is the feedback divider voltage to pin 2. This corresponds to the inverting input node of the amplifier, from Figure 9.43.

Note that in both of the cases of Figure 9.44, the guard physical connections shown are only partial—an actual layout would include all sensitive nodes within the circuit. In both the inverting and the non-inverting modes using the MINIDIP or other through-hole style package, the PCB guard traces should be located on both sides of the board, with top and bottom traces connected with several vias.

Things become slightly more complicated when using guarding techniques with the SOIC surface mount ("R") package, as the 0.05" pin spacing doesn't easily allow routing of PCB traces between the pins. But, there is still an effective guarding answer, at least for the inverting case. Figure 9.45 shows guards for the ADI "R" style SOIC package.

Note that for many single op amp devices in this SOIC "R" package, pins 1, 5, and 8 are "no connect" pins. For such instances, this means that these locations can be employed in the layout to route guard traces. In the case of the inverting mode (left), the guarding is still completely effective, with the dummy pin 1 and pin 3 serving as the grounded guard trace. This is a fully effective guard without compromise. Also, with SOIC op amps, much of the circuitry around the device will not use through-hole components. So, the guard ring may only be necessary on the op amp PCB side.

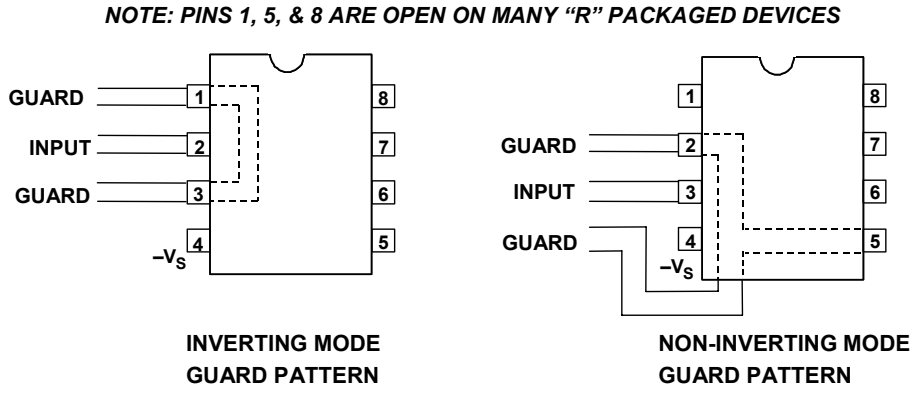


Figure 9.45: *PCB Guard Patterns for Inverting and Non-Inverting Mode Op Amps Using 8 Pin SOIC (R) Package*

In the case of the follower stage (right), the guard trace must be routed around the negative supply at pin 4, and thus pin 4 to pin 3 leakage isn't fully guarded. For this reason, a precision high impedance follower stage using an SOIC package op amp isn't generally recommended, as guarding isn't as effective for dual supply connected devices.

However, an exception to this caveat does apply to the use of a *single-supply* op amp as a non-inverting stage. For example, if the AD8551 is used, pin 4 becomes ground, and some degree of intrinsic guarding is then established by default.

Dynamic PCB Effects

Although static PCB effects can come and go with changes in humidity or board contamination, problems that most noticeably affect the dynamic performance of a circuit usually remain relatively constant. Short of a new design, washing or any other simple fixes can't fix them. As such, they can permanently and adversely affect a design's specifications and performance. The problems of stray capacitance, linked to lead and component placement, are reasonably well known to most circuit designers. Since lead placement can be permanently dealt with by correct layout, any remaining difficulty is solved by training assembly personnel to orient components or bend leads optimally.

Dielectric absorption (DA), on the other hand, represents a more troublesome and still poorly understood circuit-board phenomenon. Like DA in discrete capacitors, DA in a printed-circuit board can be modeled by a series resistor and capacitor connecting two closely spaced nodes. Its effect is inverse with spacing and linear with length.

As shown in Figure 9.46, the RC model for this effective capacitance ranges from 0.1 to 2.0 pF, with the resistance ranging from 50 to 500 MΩ. Values of 0.5 pF and 100 MΩ are most common. Consequently, circuit-board DA interacts most strongly with high-impedance circuits.

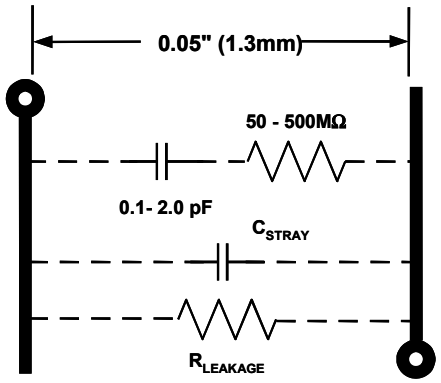


Figure 9.46: *DA Plagues Dynamic Response of PCB-Based Circuits*

PCB DA most noticeably influences dynamic circuit response, for example, settling time. Unlike circuit leakage, the effects aren't usually linked to humidity or other environmental conditions, but rather, are a function of the board's dielectric properties. The chemistry involved in producing plated-through holes seems to exacerbate the problem. If your circuits don't meet expected transient response specs, you should consider PCB DA as a possible cause.

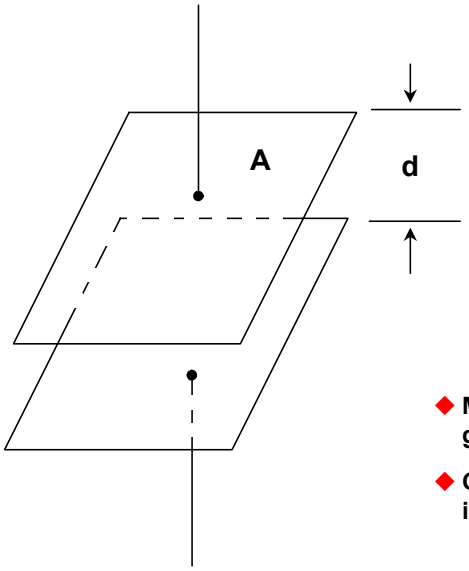
Fortunately, there are solutions. As in the case of capacitor DA, external components can be used to compensate for the effect. More importantly, surface guards that totally isolate sensitive nodes from parasitic coupling often eliminate the problem (note that these guards should be duplicated on both sides of the board, in cases of through-hole components). As noted previously, low-loss PCB dielectrics are also available at higher costs.

PCB "hook", similar if not identical to DA, is characterized by variation in effective circuit-board capacitance with frequency (see Reference 1). In general, it affects high-impedance circuit transient response where board capacitance is an appreciable portion of the total in the circuit. Circuits operating at frequencies below 10 kHz are the most susceptible. As in circuit board DA, the board's chemical makeup very much influences its effects.

Stray Capacitance

When two conductors aren't short-circuited together, or totally screened from each other by a conducting (Faraday) screen, there is a capacitance between them. So, on any PCB, there will be a large number of capacitors associated with any circuit (which may or may not be considered in models of the circuit). Where high frequency performance matters (and even dc and VLF circuits may use devices with high F_t and therefore be vulnerable to high frequency instability), it is very important to consider the effects of this stray capacitance.

Any basic textbook will provide formulas for the capacitance of parallel wires and other geometric configurations (see References 9 and 10). The example we need consider in this discussion is the parallel plate capacitor, often formed by conductors on opposite sides of a PCB. The basic diagram describing this capacitance is shown in Figure 9.47.



$$C = \frac{0.00885\ E_r\ A}{d}\ pF$$

A = plate area in mm^2

d = plate separation in mm

E_r = dielectric constant relative to air

- **Most common PCB type uses 1.5mm glass-fiber epoxy material with $E_r = 4.7$**
- **Capacity of PC track over ground plane is roughly 2.8pF/cm^2**

Figure 9.47: *Capacitance of Two Parallel Plates*

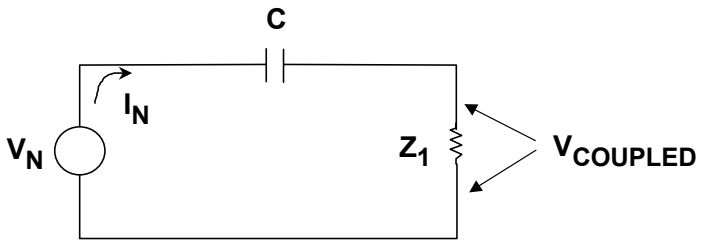
Neglecting edge effects, the capacitance of two parallel plates of area A mm^2 and separation d mm in a medium of dielectric constant E_r relative to air is $0.00885\ E_r\ A/d$ pF.

From this formula, we can calculate that for general purpose PCB material ($E_r = 4.7$, d = 1.5 mm), the capacitance between conductors on opposite sides of the board is just under 3 pF/cm^2. In general, such capacitance will be parasitic, and circuits must be designed so that it does not affect their performance.

While it is possible to use PCB capacitance in place of small discrete capacitors, the dielectric properties of common PCB substrate materials cause such capacitors to behave poorly. They have a rather high temperature coefficient and poor Q at high frequencies, which makes them unsuitable for many applications. Boards made with lower-loss dielectrics such as Teflon are expensive exceptions to this rule.

Capacitive Noise and Faraday Shields

There is a capacitance between any two conductors separated by a dielectric (air or vacuum are dielectrics). If there is a change of voltage on one, there will be a movement of charge on the other. A basic model for this is shown in Figure 9.48.



Z_1 = CIRCUIT IMPEDANCE
$Z_2 = 1/j\omega C$

$$V_{COUPLED} = V_N \left(\frac{Z_1}{Z_1 + Z_2} \right)$$

Figure 9.48: *Capacitive Coupling Equivalent Circuit Model*

It is evident that the noise voltage, $V_{COUPLED}$ appearing across Z_1, may be reduced by several means, all of which reduce noise current in Z_1. They are reduction of the signal voltage V_N, reduction of the frequency involved, reduction of the capacitance, or reduction of Z_1 itself. Unfortunately however, often none of these circuit parameters can be freely changed, and an alternate method is needed to minimize the interference. The best solution towards reducing the noise coupling effect of C is to insert a grounded conductor, also known as a *Faraday shield*, between the noise source and the affected circuit. This has the desirable effect of reducing Z_1 noise current, thus reducing $V_{COUPLED}$.

A Faraday shield model is shown by Figure 9.49. In the left picture, the function of the shield is noted by how it effectively divides the coupling capacitance, C. In the right picture the net effect on the coupled voltage across Z_1 is shown. Although the noise current I_N still flows in the shield, most of it is now diverted away from Z_1. As a result, the coupled noise voltage $V_{COUPLED}$ across Z_1 is reduced.

A Faraday shield is easily implemented and almost always successful. Thus capacitively coupled noise is rarely an intractable problem. However, to be fully effective, a Faraday shield must completely block the electric field between the noise source and the shielded circuit. It must also be connected so that the displacement current returns to its source, without flowing in any part of the circuit where it can introduce conducted noise.

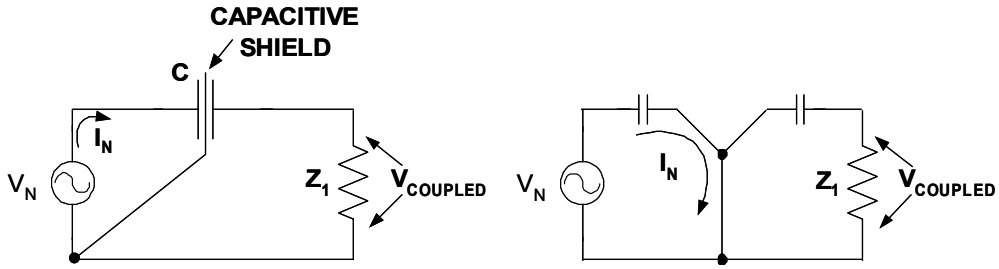


Figure 9.49: *An Operational Model of a Faraday Shield*

The Floating Shield Problem

And, it is quite important to note here—*a conductor that is intended to function as a Faraday shield must never be left floating, as this almost always increases capacity and exacerbates the noise problem*!

An example of this "floating shield" problem is seen in side-brazed ceramic IC packages. These DIP packages have a small square conducting Kovar lid soldered onto a metallized rim on the ceramic package top. Package manufacturers offer only two options: the metallized rim may be connected to one of the corner pins of the package, or it may be left unconnected.

Most logic circuits have a ground pin at one of the package corners, and therefore the lid is grounded. Alas, many analog circuits don't have a ground pin at a package corner, and the lid is left floating—acting as an antenna for noise. Such circuits turn out to be far more vulnerable to electric field noise than the same chip in a plastic DIP package, where the chip is completely unshielded.

Whenever practical, it is good practice for the user to ground the lid of any side brazed ceramic IC where the lid is not grounded by the manufacturer, thus implementing an *effective* Faraday shield. This can be done with a wire soldered to the lid (this will not damage the device, as the chip is thermally and electrically isolated from the lid). If soldering to the lid is unacceptable, a grounded phosphor-bronze clip or conductive paint from the lid to the ground pin may be used to make the ground connection,.

A safety note is appropriate at this point. Never attempt to ground such a lid without first verifying that it is unconnected. Occasionally device types are found with the lid connected to a power supply rather than to ground!

A case where a Faraday shield is impractical is between IC chip bondwires. This can have important consequences, as the stray capacitance between chip bondwires and associated leadframes is typically ≈ 0.2 pF, with observed values generally between 0.05 and 0.6 pF.

Buffering ADCs Against Logic Noise

If we have a high resolution data converter (ADC or DAC) connected to a high speed data bus which carries logic noise with a 2-5 V/ns edge rate, this noise is easily connected

to the converter analog port via stray capacitance across the device. Whenever the data bus is active, intolerable amounts of noise are capacitively coupled into the analog port, thus seriously degrading performance.

This particular effect is illustrated by the diagram of Figure 9.50, where multiple package capacitors couple noisy edge signals from the data bus into the analog input of an ADC.

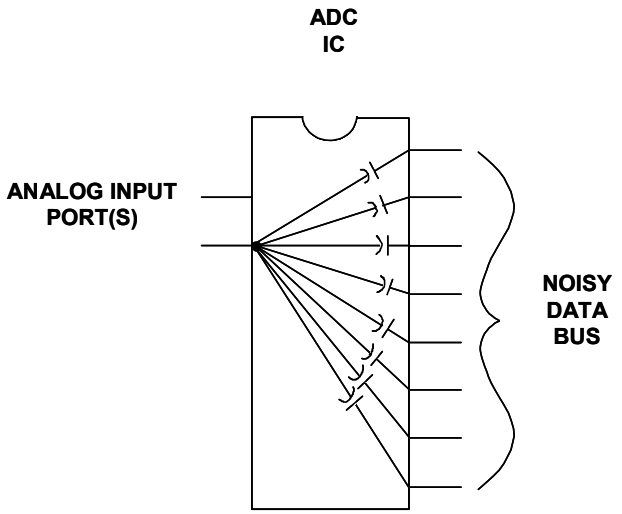
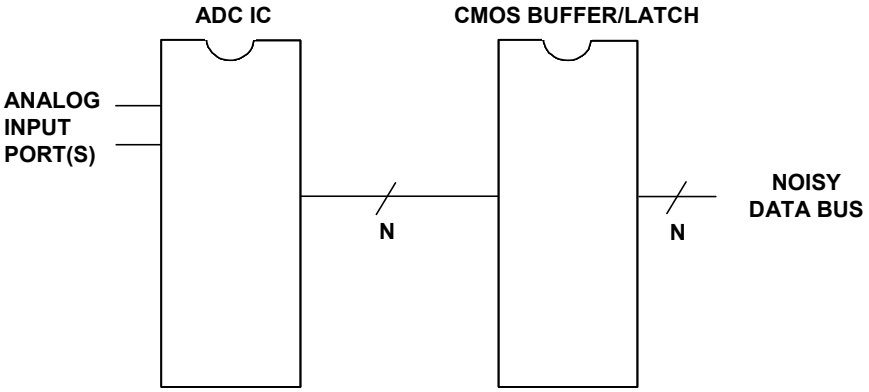


Figure 9.50: *A High Speed ADC IC Sitting on a Fast Data Bus Couples Digital Noise into the Analog Port, Thus Limiting Performance*

Present technology offers no cure for this problem, within the affected IC device itself. The problem also limits performance possible from other broadband monolithic mixed signal ICs with single-chip analog and digital circuits. Fortunately, this coupled noise problem can be simply avoided, by *not* connecting the data bus directly to the converter.

Instead, *use a CMOS latched buffer as a converter-to-bus interface*, as shown by Figure 9.51. Now the CMOS buffer IC acts as a Faraday shield, and dramatically reduces noise coupling from the digital bus. This solution costs money, occupies board area, reduces reliability (very slightly), consumes power, and it complicates the design—but it does improve the signal-to-noise ratio of the converter! The designer must decide whether it is worthwhile for individual cases, but in general it is highly recommended.

Bus switches can also be utilized to isolate data lines from buses as described later in this chapter.



- THE OUTPUT BUFFER/LATCH ACTS AS A FARADAY SHIELD BETWEEN "N" LINES OF A FAST, NOISY DATA BUS AND A HIGH PERFORMANCE ADC.
- THIS MEASURE ADDS COST, BOARD AREA, POWER CONSUMPTION, RELIABILITY REDUCTION, DESIGN COMPLEXITY, AND MOST IMPORTANTLY, *IMPROVED PERFORMANCE!*

Figure 9.51: *A High Speed ADC IC Using a CMOS Buffer/Latch at the Output Shows Enhanced Immunity of Digital Data Bus Noise*

REFERENCES:
9.2 PC BOARD DESIGN ISSUES

1. W. Doeling, W. Mark, T. Tadewald, and P. Reichenbacher, "Getting Rid of Hook: The Hidden PC-Board Capacitance," **Electronics,** October 12, 1978, p 111-117.

2. Alan Rich, "Shielding and Guarding", **Analog Dialogue,** Vol. 17 N0. 1, 1983, pp. 8.

3. Ralph Morrison, **Grounding and Shielding Techniques, 4th Edition**, John Wiley, Inc., 1998, ISBN: 0471245186.

4. Henry W. Ott, **Noise Reduction Techniques in Electronic Systems, 2nd Edition**, John Wiley, Inc., 1988, ISBN: 0-471-85068-3.

5. Paul Brokaw, "An IC Amplifier User's Guide to Decoupling, Grounding and Making Things Go Right for a Change", **Analog Devices AN202**.

6. Paul Brokaw, "Analog Signal-Handling for High Speed and Accuracy," **Analog Devices AN342**.

7. Paul Brokaw and Jeff Barrow, "Grounding for Low- and High-Frequency Circuits," **Analog Devices AN345.**

8. Jeff Barrow, "Avoiding Ground Problems in High Speed Circuits," **RF Design**, July 1989.

9. B. I. & B. Bleaney, **Electricity & Magnetism**, Oxford at the Clarendon Press, 1957, pp 23, 24, & 52.

10. G. W. A. Dummer, H. Nordenberg, **Fixed and Variable Capacitors**, McGraw-Hill, 1960, pp 11-13.

11. William C. Rempfer, *Get All the Fast ADC Bits You Pay For*, **Electronic Design, Special Analog Issue**, June 24, 1996, p.44.

12. Mark Sauerwald, *Keeping Analog Signals Pure in a Hostile Digital World*, **Electronic Design, Special Analog Issue**, June 24, 1996, p.57.

13. Jerald Grame and Bonnie Baker, *Design Equations Help Optimize Supply Bypassing for Op Amps*, **Electronic Design, Special Analog Issue**, June 24, 1996, p.9.

14. Jerald Grame and Bonnie Baker, *Fast Op Amps Demand More Than a Single-Capacitor Bypass*, **Electronic Design, Special Analog Issue**, November 18, 1996, p.9.

15. Walt Kester and James Bryant, *Grounding in High Speed Systems*, **High Speed Design Techniques**, Analog Devices, 1996, Chapter 7, p. 7-27.

16. Jeffrey S. Pattavina, *Bypassing PC Boards: Thumb Your Nose at Rules of Thumb*, **EDN**, Oct. 22, 1998, p.149.

17. Howard W. Johnson and Martin Graham, **High-Speed Digital Design**, PTR Prentice Hall, 1993, ISBN: 0133957241.

18. Walt Kester, *A Grounding Philosophy for Mixed-Signal Systems*, **Electronic Design Analog Applications Issue**, June 23, 1997, p. 29.

19. Ralph Morrison, **Solving Interference Problems in Electronics**, John Wiley, 1995.

20. C. D. Motchenbacher and J. A. Connelly, **Low Noise Electronic System Design**, John Wiley, 1993.

21. Crystal Oscillators: MF Electronics, 10 Commerce Drive, New Rochelle, NY, 10801, 914-576-6570.

22. Crystal Oscillators: Wenzel Associates, Inc., 2215 Kramer Lane, Austin, Texas USA 78758, 512-835-2038, http://www.wenzel.com.

23. Mark Montrose, **EMC and the Printed Circuit Board**, IEEE Press, 1999 (IEEE Order Number PC5756).

ACKNOWLEDGEMENTS:

Portions of this section were adapted from Doug Grant and Scott Wurcer, "Avoiding Passive Component Pitfalls", originally published in **Analog Dialogue 17-2**, 1983.

SECTION 9.3: ANALOG POWER SUPPLY SYSTEMS

Walt Jung, Walt Kester

Analog circuits have traditionally been powered from well-regulated, low noise linear power supplies. This type of power system is typically characterized by medium-to-low power conversion efficiency. Such linear regulators usually excel in terms of self-generated and radiated noise components. If the designer's life were truly simple, it might continue with such familiar designs offering good performance and minimal side effects.

But, the designer's life is hardly so simple. Modern systems may allow using linear regulators, but multiple output levels and/or polarities are often required. There may also be some additional requirements set for efficiency, which may dictate the use of dc-dc conversion techniques, and, unfortunately, their higher associated noise output.

This section addresses power supply design issues for analog systems (including op amps, analog multiplexers, ADCs, DACs, etc.), taking into account the regulator types most likely to be used. The primary dc power sources are assumed to be either rectified and smoothed ac sources (i.e., mains derived), a battery stack, or a switching regulator output. The latter example could be fed from either a battery or a mains-derived dc source.

As noted in Figure 9.52, linear mode regulation is generally recommended as an optimum starting point in all instances (first bullet). Nevertheless, in some cases, a degree of hybridization between fully linear and switching mode regulation may be required (second bullet). This could be either for efficiency or other diverse reasons.

- **High performance analog power systems use *linear regulators*, with primary power derived from:**
  - **AC line power**
  - **Battery power systems**
  - **DC- DC power conversion systems**
- ***Switching regulators* should be avoided if at all possible, but if not…**
  - **Apply noise control techniques**
  - **Use quality layout and grounding**
  - **Be aware of EMI**

Figure 9.52: *Regulation Priorities for Analog Power Supply Systems*

Whenever switching-type regulators are involved in powering precision analog circuits, noise control is very likely to be a design issue. Therefore some focus of this section is on minimizing noise when using switching regulators.

Linear IC Regulation

Linear IC voltage regulators have long been standard power system building blocks. After an initial introduction in 5-V logic voltage regulator form, they have since expanded into other standard voltage levels spanning from 3 to 24 V, handling output currents from as low as 100 mA (or less) to as high as 5 A (or more). For several good reasons, linear style IC voltage regulators have been valuable system components since the early days. As mentioned above, a basic reason is the relatively low noise characteristic vis-à-vis the switching type of regulator. Others are a low parts count and overall simplicity compared to discrete solutions. But, because of their power losses, these linear regulators have also been known for being relatively inefficient. Early generation devices (of which many are still available) required 2V or more of unregulated input above the regulated output voltage, making them lossy in power terms.

More recently however, linear IC regulators have been developed with more liberal (i.e., lower) limits on minimum input-output voltage. This voltage, known more commonly as *dropout* voltage, has led to what is termed the *Low Drop Out* regulator, or more simply, the LDO. Dropout voltage (V_{MIN}) is defined simply as that minimum input-output differential where the regulator undergoes a 2% reduction in output voltage. For example, if a nominal 5.0-V LDO output drops to 4.9 V (–2%) under conditions of an input-output differential of 0.5 V, by this definition the LDO's dropout voltage is 0.5 V.

Dropout voltage is extremely critical to a linear regulator’s power efficiency. The lower the voltage allowable across a regulator while still maintaining a regulated output, the less power the regulator dissipates as a result. A low regulator dropout voltage is the key to this, as it takes a lower dropout to maintain regulation as the input voltage lowers. In performance terms, the bottom line for LDOs is simply that more useful power is delivered to the load and less heat is generated in the regulator. LDOs are key elements of power systems providing stable voltages from batteries, such as portable computers, cellular phones, etc. This is because they maintain a regulated output down to lower points on the battery’s discharge curve. Or, within classic mains-powered raw dc supplies, LDOs allow lower transformer secondary voltages, reducing system shutdowns under brownout conditions, as well as allowing cooler operation.

Some Linear Voltage Regulator Basics

A brief review of three terminal linear IC regulator fundamentals is necessary before understanding the LDO variety. Most (but not all) of the general three terminal regulator types available today are *positive leg, series style* regulators. This simply means that they control the regulated voltage output by means of a pass element in series with the positive unregulated input. And, although they are fewer in number, there are also *negative leg* series style regulators, which operate in a fashion complementary to the positive units.

A basic hookup diagram of a three terminal regulator is shown in Figure 9.53. In terms of basic functionality, many standard voltage regulators operate in a series mode, three-terminal form, just as shown here. As can be noted from this figure, the three I/O terminals are V_{IN}, GND (or Common), and V_{OUT}. Note also that this regulator block, in the absence of any assigned voltage polarity, could in principle be a positive type

regulator. Or, it might also be a negative style of voltage regulator—the principle is the same for both— a common terminal, as well as input and output terminals.

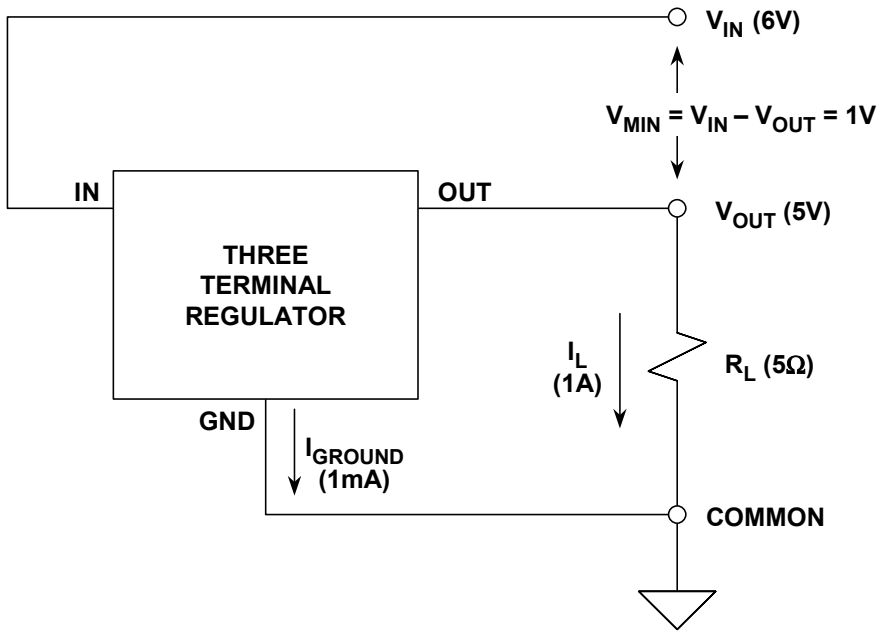


Figure 9.53: *A Basic Three Terminal Regulator Hookup (Either Positive or Negative)*

In operation, there are two power components which get dissipated in the regulator, one a function of $V_{IN} - V_{OUT}$ and I_L, plus a second which is a function of V_{IN} and Iground. The first of these is usually dominant. Analysis of the situation will reveal that as the dropout voltage V_{MIN} is reduced, the regulator is able to deliver a higher percentage of the input power to the load, and is thus more efficient, running cooler and saving power. This is the core appeal of the modern LDO type of regulator (see Chapter 7 of this book and Reference 1).

A more detailed look within a typical regulator block diagram reveals a variety of elements, as is shown in Figure 9.54. Note that all regulators will contain those functional components connected via solid lines. The connections shown dotted indicate options, which might be available when more than three I/O pins are available.

In operation, a voltage reference block produces a stable voltage V_{REF}, which is almost always a voltage based on the bandgap voltage of silicon, typically ~1.2 V (see Reference 2). This allows output voltages of 3 V or more from supplies as low as 5 V. This voltage drives one input of an error amplifier, with the second input connected to the divider, R1-R2. The error amplifier drives the pass device, which in turn controls the output. The resulting regulated voltage is then simply:

$$V_{OUT} = V_{REF}\left(1 + \frac{R1}{R2}\right). \qquad \text{Eq. 9.5}$$

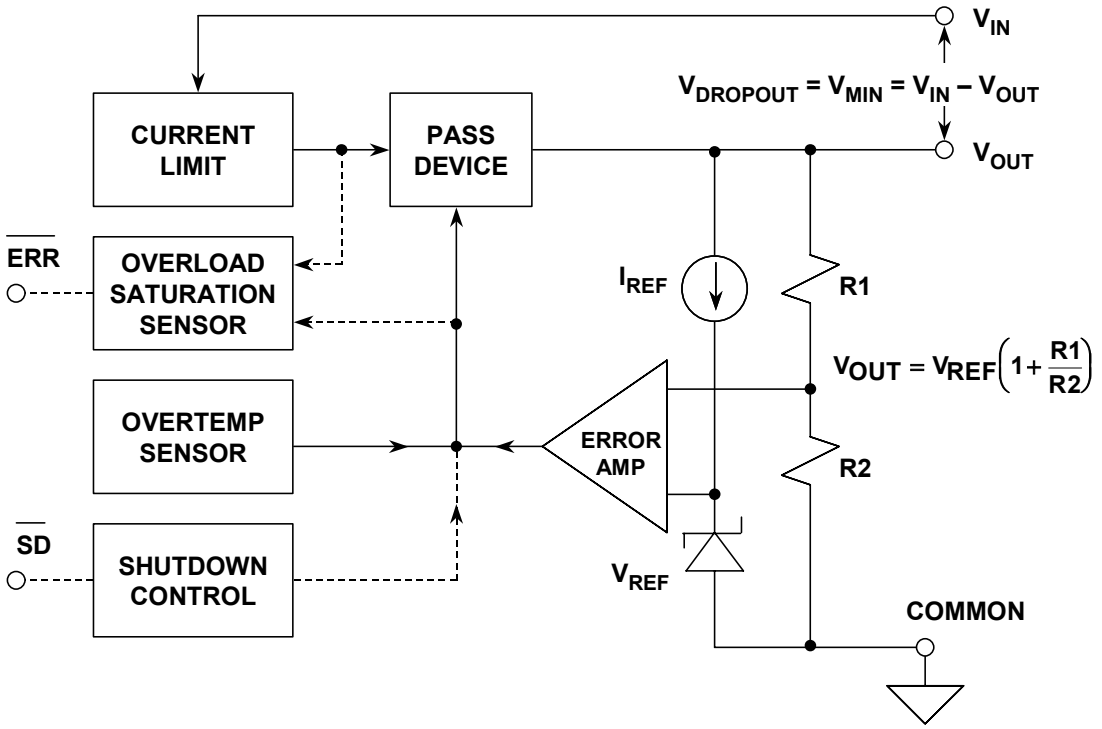


Figure 9.54: *Block Diagram of a Voltage Regulator*

Pass Devices

The pass device is a foremost regulator part, and the type chosen here has a major influence on almost all regulator performance issues. Most notable among these is dropout voltage, V_{MIN}. Analysis shows the use of an *inverting* mode pass transistor allows the pass device to be effectively saturated, thus minimizing the associated voltage losses. Therefore this factor makes the two most desirable pass devices for LDO use a PNP bipolar, or a PMOS transistor. These device types achieve the lowest levels of $V_{IN} - V_{OUT}$ required for LDO operation. In contrast, NPN bipolars are poor as pass devices in terms of low dropout, particularly when they are Darlington connected.

Standard fixed-voltage IC regulator architectures illustrate this point regarding pass devices. For example, the fixed-voltage LM309 5-V regulators and family derivatives such as the 7805, 7815 et. al., (and their various low and medium current alternates) are poor in terms of dropout voltage. These designs use a Darlington pass connection, not known for low dropout (~1.5 V typical), or for low quiescent current (~5 mA).

±15-V Regulator Using Adjustable Voltage ICs

Later developments in references and three-terminal regulation techniques led to the development of the *voltage-adjustable* regulator. The original IC to employ this concept was the LM317, a positive regulator. The device produces a fixed reference voltage of 1.25 V, appearing between the V_{OUT} and ADJ pins of the IC. External scaling resistors set up the desired output voltage, adjustable in the range of 1.25-30 V. A complementary device, the LM337, operates in similar fashion, regulating negative voltages.

An application example using standard *adjustable* three terminal regulators to implement a ±15-V linear power supply is shown in Figure 9.55. This is a circuit as might be used for powering traditional op amp supply rails. It is capable of better line regulation performance than would an otherwise similar circuit, using standard fixed-voltage regulator devices, such as for example 7815 and 7915 ICs. However, in terms of power efficiency it isn't outstanding, due to the use of the chosen ICs, which require 2 V or more of headroom for operation.

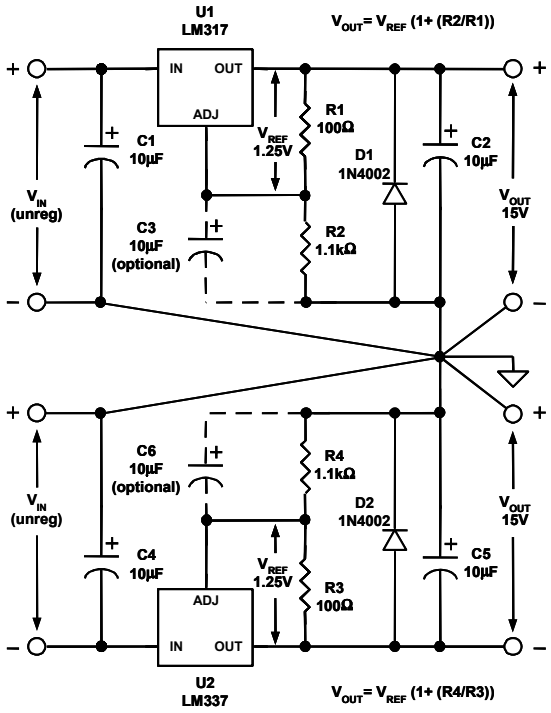


Figure 9.55: *A Classic ±15V, 1 A Linear Supply Regulator Using Adjustable Voltage Regulator ICs*

In the upper portion of this circuit an LM317 adjustable regulator is used, with R2 and R1 chosen to provide a 15-V output at the upper output terminal. If desired, R2 can easily be adjusted for other output levels, according to the figure's V_{OUT} equation. Resistor R1 should be left fixed, as it sets the minimum regulator drain of 10 mA or more.

In this circuit, capacitors C1 and C2 should be tantalum types, and R1-R2 metal films. C3 is optional, but is highly recommended if the lowest level of output noise is desired. The normally reverse biased diode D1 provides a protective output clamp, for system cases where the output voltage would tend to reverse, if one supply should fail. The circuit operates from a rectified and filtered ac supply at V_{IN}, polarized as shown. The output current is determined by choosing the regulator IC for appropriate current capability. To implement the negative supply portion, the sister device to the LM317 is used, the LM337. The bottom circuit section thus mirrors the operation of the upper, delivering a negative 15V at the lowest output terminal. Programming of the LM337 for output voltage is similar to that of the LM317, but uses resistors R4 and R3. R4 should be used to adjust the voltage, with R3 remaining fixed. C6 is again optional, but is recommended for reasons of lowest noise.

Low Dropout Regulator Architectures

In contrast to traditional three terminal regulators with Darlington or single-NPN pass devices, low dropout regulators employ lower voltage threshold pass devices. This basic operational difference allows them to operate effectively down to a range of 100-200 mV in terms of their specified V_{MIN}. In terms of use within a system, this factor can have fairly significant operational advantages.

An effective implementation of some key LDO features is contained in the Analog Devices series of anyCAP® LDO regulators. Devices of this ADP33xx series are so named for their relative insensitivity to the output capacitor, in terms of both its size and ESR. Available in power efficient packages such as the ADI Thermal Coastline (and other thermally enhanced packages), they come in both stand-alone LDO and LDO controller forms (used with an external PMOS FET). They also offer a wide span of fixed output voltages from 1.5 to 5 V, with rated current outputs up to 1500 mA. User-adjustable output voltage versions are also available. A basic simplified diagram for the family is shown schematically in Figure 9.56.

One of the key differences in the ADP33xx LDO series is the use of a high gain vertical PNP pass device, Q1, allowing typical dropout voltages for the series to be on the order of 1mV/mA for currents of 200 mA or less.

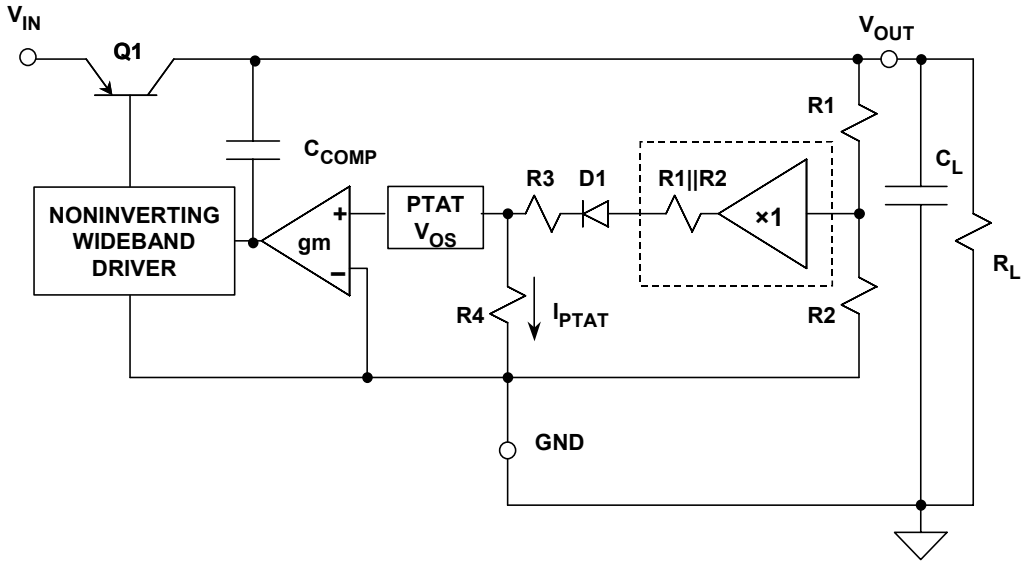


Figure 9.56: *The ADP33xx anyCAP® LDO Architecture Has Both DC and AC Performance Advantages*

In circuit operation, V_{REF} is defined as a reference voltage existing at the output of a zero impedance divider of ratio R1/R2. In the figure, this is depicted symbolically by the (dotted) unity gain buffer amplifier fed by R1/R2, which has an output of V_{REF}. This reference voltage feeds into a series connection of (dotted) R1||R2, then actual components D1, R3, R4, etc. The regulator output voltage is:

$$V_{OUT} = V_{REF}\left(1 + \frac{R1}{R2}\right). \qquad \text{Eq. 9.6}$$

In the various devices of the ADP33xx series, the R1-R2 divider is adjusted to produce standard output voltages of 1.5, 1.8, 2.5, 2.7, 2.75, 2.77, 2.85, 2.9, 3.0, 3.15, 3.2, 3.3, 3.6, and 5.0 V. The regulator behaves as if the entire error amplifier has simply an offset voltage of V_{REF} volts, as seen at the output of a conventional R1-R2 divider.

While the above described dc performance enhancements of the ADP33xx series are worthwhile, more dramatic improvements come in areas of ac-related performance. Capacitive loading and the potential instability it brings is a major deterrent to easy LDO applications. One method of providing some measure of immunity to variation in an amplifier response pole is the use of a frequency compensation technique called *pole splitting*. In the Figure 9.56 circuit, C_{COMP} functions as the pole splitting capacitor, and provides benefits of a buffered, C_L independent single-pole response. As a result, frequency response is dominated by the regulator's internal compensation, and becomes relatively immune to the value and ESR of load capacitor C_L.

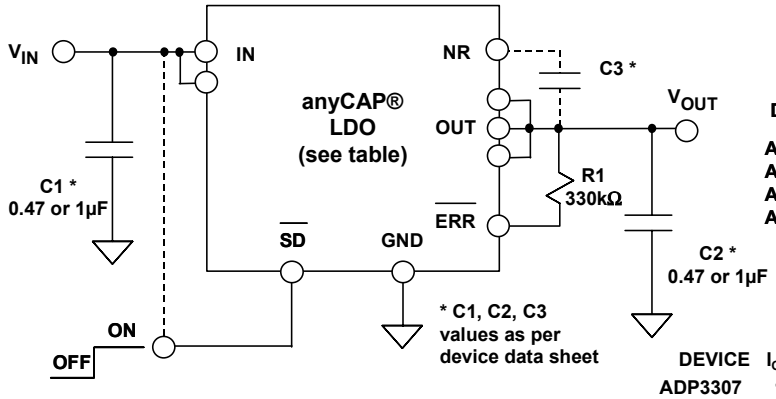
This feature makes the design tolerant of virtually any output capacitor type. C_L, the load capacitor, can be as low as 0.47 µF, and it can also be a multi-layer ceramic capacitor (MLCC) type, allowing a very small physical size for the entire regulation function.

Fixed-Voltage, 50/100/200/500/1000/1500 mA LDO Regulators

A basic regulator application diagram common to various fixed voltage devices of the ADP33xx device series is shown by Figure 9.57. Operation of the various pins and internal functions is discussed below. Note that all pins and all functions are not available on all parts in the series, and individual data sheets should be consulted.

This circuit is a general one, illustrating common points. For example, the ADP33xx is a 50-mA basic LDO regulator device, designed for those fixed output voltages as noted. An actual ADP3300 device ordered would be ADP3300ART-YY, where the "YY" is a voltage designator suffix such as 2.7, 3, 3.2, 3.3, or 5, for the respective table voltages. The "ART" portion of the part number designates the package (SOT23 6-lead). To produce 5V from the circuit, use the ADP3300ART-5. Similar comments apply to the other devices, insofar as part numbering. For example, an ADP3301AR-5 depicts an SO-8 packaged 100-mA device, producing 5-V output.

In operation, the circuit produces rated output voltage for loads under the max current limit, for input voltages above $V_{OUT} + V_{MIN}$ (where V_{MIN} is the dropout voltage for the specific device used, at rated current). The circuit is ON when the shutdown input (if available on the particular device selected) is in a HIGH state, either by a logic HIGH control input to the $\overline{SD}$ pin, or by simply tying this pin to V_{IN} (shown dotted). When $\overline{SD}$ is LOW or grounded, the regulator shuts down, and draws a minimum quiescent current.



OUTPUT TABLE

DEVICE	I_{OUT}(mA)	V_{OUT}(V)
ADP3300	50	2.7, 3, 3.2, 3.3, 5
ADP3301	100	2.7, 3, 3.2, 3.3, 5
ADP3303	200	2.7, 3, 3.2, 3.3, 5
ADP3303A	200	ADJ. 2.2 - 10

NOTE: MULTIPLE INPUT / OUTPUT PINS, NR, SD, ERR, NOT AVAILABLE ON ALL PARTS

DEVICE	I_{OUT}(mA)	V_{OUT}(V)
ADP3307	100	2.7, 3, 3.2, 3.3
ADP3308	50	2.7, 2.85, 2.9, 3, 3.3, 3.6
ADP3309	100	2.7, 2.85, 2.9, 3, 3.3, 3.6
ADP3330	200	2.5, 2.75, 2.85, 3, 3.3, 3.6, 5
ADP3331	200	ADJ. 1.5 - 10
ADP3333	300	1.5, 1.8, 2.5, 2.77, 3, 3.15, 3.3, 5
ADP3334	500	ADJ. 1.5 - 10
ADP3335	500	1.8, 2.5, 2.85, 3.3, 5
ADP3336	500	ADJ. 1.5 - 10
ADP3338	1000	1.8, 2.5, 2.85, 3.3, 5
ADP3339	1500	1.8, 2.5, 2.85, 3.3, 5

Figure 9.57: *A Basic LDO Regulator Hookup Useful by Device Selection From 50 to 1500mA, At Fixed or Adjustable Voltages Per Table*

The anyCAP regulator devices maintain regulation over a wide range of load, input voltage and temperature conditions. Most devices have a combined error band of ±1.4% (or less). When an overload condition is detected, the open collector $\overline{\text{ERR}}$ goes to a LOW state (if available on the particular device selected). R1 is a pullup resistor for the $\overline{\text{ERR}}$ output. This resistor can be eliminated if the load provides a pullup current.

C3, connected between the OUT and NR pins, can be used for an optional noise reduction (NR) feature (if available on the particular device selected). This is accomplished by bypassing a portion of the internal resistive divider, which reduces output noise ~10 dB. When exercised, only the recommended low leakage capacitors as specific to a particular part should be used.

The C1 input and C2 output capacitors should be selected as either 0.47 or 1-µF values respectively, again, as per the particular device used. For most devices of the series 0.47 µF suffices, but the ADP3335 uses the 1-µF values. Larger capacitors can also be used, and will provide better transient performance.

Heat sinking of device packages with more than 5 pins is enhanced, by use of multiple IN and OUT pins. All of the pins available should therefore be used in the PCB design, to minimize layout thermal resistance.

Adjustable Voltage, 200-mA LDO Regulator

In addition to the fixed output voltage LDO devices discussed above, adjustable versions are also available, to realize non-standard voltages. The ADP3331 is one such device, and it is shown in Figure 9.58, configured as a 2.8-V output, 200-mA LDO application.

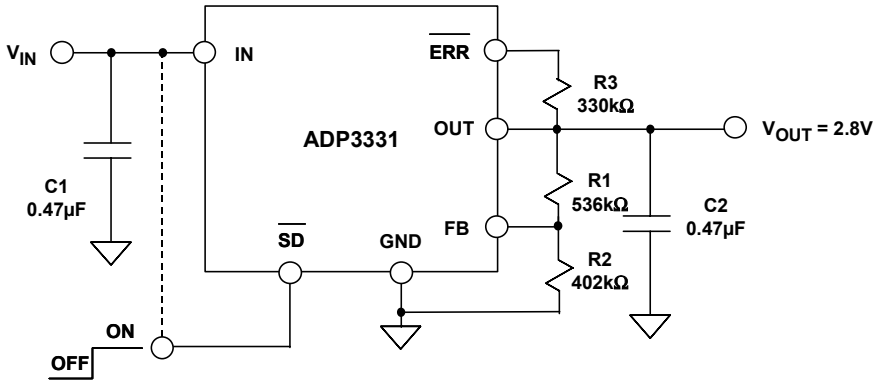


Figure 9.58: *An Adjustable 200mA LDO Regulator Set Up for a 2.8-V Output*

The ADP3331 is generally similar to other anyCAP LDO parts, with two notable exceptions. It has a lower quiescent current (~34 µA when lightly loaded) and most importantly, the output voltage is user-adjustable. As noted in the circuit, R1 and R2 are external precision resistors used to define the regulator operating voltage.

The output of this regulator is V_{OUT}, which is related to feedback pin FB voltage V_{FB} as:

$$V_{OUT} = V_{FB}\left(1 + \frac{R1}{R2}\right) \quad , \qquad \text{Eq. 9.7}$$

where V_{FB} is 1.204 V. Resistors R1 and R2 program V_{OUT}, and their parallel equivalent should be kept close to 230 kΩ for best stability. To select R1 and R2, first calculate their ideal values, according to the following two expressions:

$$R1 = 230\left(\frac{V_{OUT}}{V_{FB}}\right)k\Omega \qquad \text{Eq. 9.8}$$

$$R2 = \frac{230}{\left(1 + \frac{V_{FB}}{V_{OUT}}\right)}k\Omega \qquad \text{Eq. 9.9}$$

In the example circuit, V_{OUT} is 2.8 V, which yields R1 = 534.9 kΩ, and R2 = 403.5 kΩ. As noted in the figure, closest standard 1% values are used, which provides an output of 2.8093 V (perfect resistors assumed). In practice, the resistor tolerances should be added to the ±1.4% tolerance of the ADP3331 for an estimation of overall error.

To complement the above-discussed anyCAP series of standalone LDO regulators, there is the LDO *regulator controller*. The regulator controller IC picks up where the standalone regulator stops for either load current or power dissipation, using an external PMOS FET pass device. As such, the current capability of the LDO can be extended to several amps. An LDO regulator controller application is shown later in this discussion.

These application examples above illustrate a subset of the entire anyCAP family of LDOs. Further information on this series of standalone and regulator controller LDO devices can be found in the references at the end of the section.

Charge-Pump Voltage Converters

Another method for developing supply voltage for op amp systems employs what is known as a *charge-pump* circuit (also called switched capacitor voltage conversion). Charge-pump voltage converters accomplish energy transfer and voltage conversion using charges stored on capacitors, thus the name, charge-pump.

Using switching techniques, charge-pumps convert supply voltage of one polarity to a higher or lower voltage, or to an alternate polarity (at either higher or lower voltage). This is accomplished with only an array of low resistance switches, a clock for timing, and a few external storage capacitors to hold the charges being transferred in the voltage conversion process. No inductive components are used, thus EMI generation is kept to a minimum. Although relatively high currents are switched internally, the high current switching is localized, and therefore the generated noise is not as great as in inductive type switchers. With due consideration towards component selection, charge-pump converters can be implemented with reasonable noise performance.

The two common charge-pump voltage converters are the *voltage inverter* and the *voltage doubler* circuits. In a voltage inverter, a charge pump capacitor is charged to the input voltage during the first half of the switching cycle. During the second half of the switching cycle the input voltage stored on the charge pump capacitor is inverted, and is applied to an output capacitor and the load. Thus the output voltage is essentially the negative of the input voltage, and the average input current is approximately equal to the output current. The switching frequency impacts the size of the external capacitors required, and higher switching frequencies allow the use of smaller capacitors. The duty cycle—defined as the ratio of charge pump charging time to the entire switching cycle time—is usually 50%, which yields optimal transfer efficiency.

A voltage doubler works similarly to the inverter. In this case the pump capacitor accomplishes a voltage doubling function. In the first phase it is charged from the input, but in the second phase of the cycle it appears in series with the output capacitor. Over time, this has the effect of doubling the magnitude of the input voltage across the output capacitor and load. Both the inverter and voltage doubler circuits provide no voltage regulation in basic form. However, techniques exist to add regulation (discussed below).

There are advantages and disadvantages to using charge-pump techniques, compared to inductor-based switching regulators. An obvious key advantage is the elimination of the inductor and the related magnetic design issues. In addition, charge-pump converters typically have relatively low noise and minimal radiated EMI. Application circuits are simple, and usually only two or three external capacitors are required. Because there are no inductors, the final PCB height can generally be made smaller than a comparable inductance-based switching regulator. Charge-pump inverters are also low in cost, compact, and capable of efficiencies greater than 90%. Obviously, current output is

limited by the capacitor size and the switch capacity. Typical IC charge-pump inverters have 150-mA maximum outputs.

On their downside, charge-pump converters don't maintain high efficiency for a wide voltage range of input to output, unlike inductive switching regulators. Nevertheless, they are still often suitable for lower current loads where any efficiency disadvantages are a small portion of a larger system power budget. A summary of general charge-pump operating characteristics is shown in Figure 9.59.

- **No Inductors!**
- **Minimal Radiated EMI**
- **Simple Implementation: 2 External Capacitors, 1 Diode (for Doubler), Input Capacitor**
- **Efficiency > 90% Achievable**
- **Low Cost, Compact, Low Profile (Height)**
- **Optimized for Inverting or Doubling Supply Voltage with Output Regulation: ADP3605, ADP3607**
- **Inverter/Triplers with Three Outputs from +3V Input: ADM8830, ADM8839, ADM8840**

Figure 9.59: *Some General Charge-Pump Characteristics*

An example of charge-pump applicability is the voltage inverter function. Inverters are often useful where a relatively low current negative voltage (i.e., –3 V) is required, in addition to a primary positive voltage (such as 5 V). This may occur in a single supply system, where only a few high performance parts require the negative voltage. Similarly, voltage doublers (and triplers) are useful in low current applications, where a voltage greater than a primary supply voltage is required. Both regulated and unregulated charge pump voltage inverters and doublers are available depending upon the particular application.

Regulated Output Charge-Pump Voltage Converters

Adding regulation to a simple charge-pump voltage converter function greatly enhances its usefulness for most applications. There are several techniques for adding regulation to a charge-pump converter. The most straightforward is to follow the charge-pump inverter/doubler with an LDO regulator. The LDO provides the regulated output, and can also reduce the charge-pump converter's ripple. This approach, however, adds complexity and reduces the available output voltage by the dropout voltage of the LDO (~200 mV). These factors may or may not be a disadvantage.

By far the simplest and most effective method for achieving regulation in a charge-pump voltage converter is to simply use a charge-pump design with an internal error amplifier, to control the on-resistance of one of the switches.

This method is used in the ADP3605 voltage inverter and the ADP3607 voltage doubler, devices offering regulated outputs for positive input voltage ranges. The output is sensed and fed back into the device via a sensing pin, V_{SENSE}. Key features of the series are good output regulation, 5% in the ADP3605, and a high switching frequency of 250 kHz, good for both high efficiency and small component size.

An simplified functional diagram of the ADP3607 voltage doubler IC from this series is shown in Figure 9.60. The application circuit shown in Figure 9.61 is a 3-V to 5-V doubler, with the output regulated ±5% for currents up to 50 mA. In normal operation, the SHUTDOWN pin is connected to ground. Alternately, a logic HIGH at this pin shuts the device down to a standby current of 150 µA.

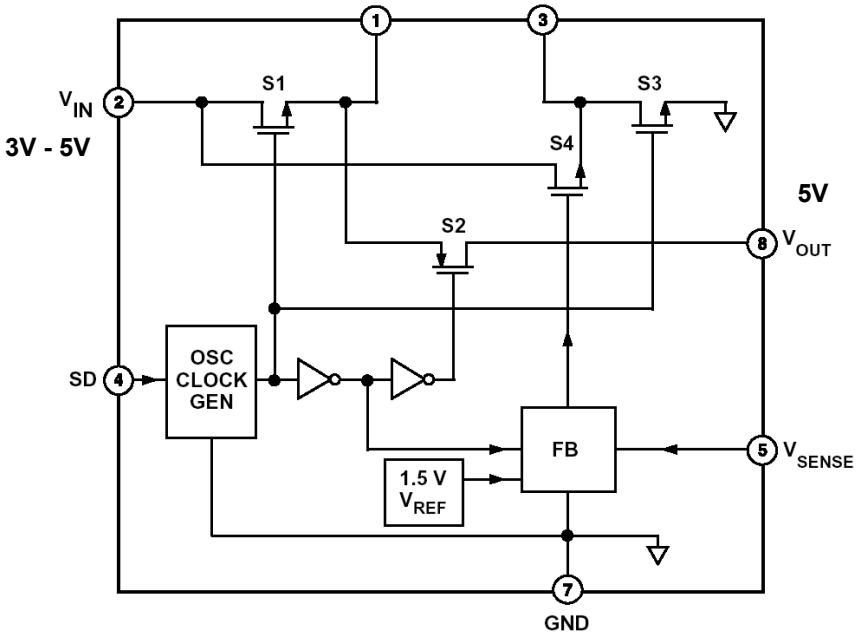


Figure 9.60: *ADP3607 Regulated 5-V, 50-mA Output Charge Pump Doubler*

The capacitors for C_{IN}, C_P, and C_O should have ESRs of less than 150 mΩ and should be 10 µF. However, 4.7 µF can be used at the expense of slightly higher output ripple voltage. C_P is the most critical of the three, because of its higher current flow. The tantalum type listed is recommended for lowest output ripple.

With values as shown, typical output ripple voltage ranges up to approximately 30 mV as the output current varies over the 50-mA range.

These application examples illustrate a subset of the entire charge-pump IC family. Other charge pumps are available, including regulated charge pumps specifically for TFT displays with three output voltages (+5 V, +15 V, and –15 V) are available. For further information on these and other devices consult http://www.analog.com.

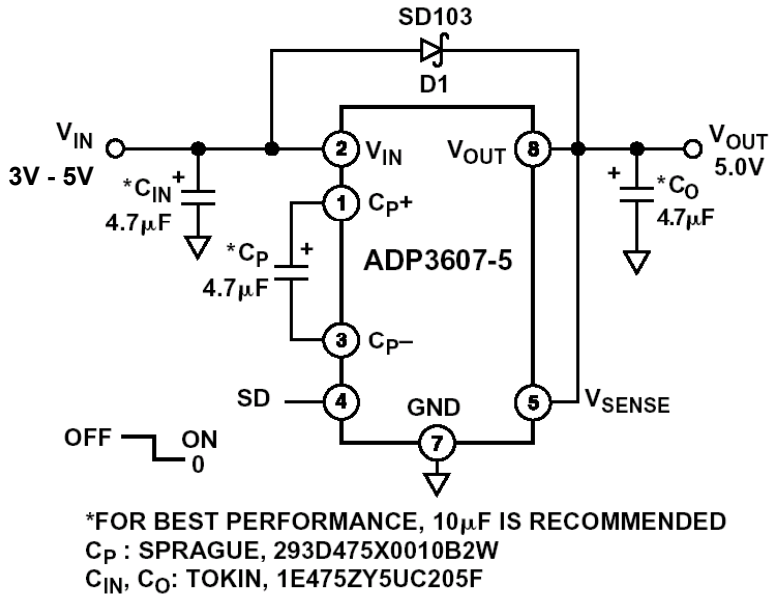


Figure 9.61: *ADP3607-5 Charge Pump Application Circuit*

Linear Post Regulator for Switching Supplies

Another powerful noise reduction option which can be utilized in conjunction with a switching type supply is the option of a *linear post regulator* stage. This is at best an LDO type of regulator, chosen for the desired clean analog voltage level and current. It is preceded by a switching stage, which might be a buck or boost type inductor-based design, or it may also be a charge-pump. The switching converter allows the overall design to be more power-efficient, and the linear post regulator provides clean regulation at the load, reducing the noise of the switcher. This type of regulator can also be termed *hybrid regulation*, since it combines both switching and linear regulation concepts.

An example circuit is shown in Figure 9.62, which features a 3.3-V/1-A low noise, analog-compatible regulator. It operates from a nominal 9V supply, using a buck or step-down type of switching regulator, as the first stage at the left. The switcher output is set for a few hundred mV above the desired final voltage output, minimizing power in the LDO stage at the right. This feature may eliminate need for a heat sink on the LDO pass device.

In this example the 1148 IC switcher is set up for a 3.75-V output by R1-R2, but in principle, this voltage can be anything suitable to match the headroom of the companion LDO (within specification limits, of course). In addition, the principle extends to any LDO devices and other current levels, and other switching regulators. The ADP3310-3.3 is a fixed-voltage LDO controller, driving a PMOS FET pass device, with a 3.3-V output.

The linear post regulation stage provides both noise-reduction (in this case about 14 dB), as well as good dc regulation. To realize best results, good grounding practices must be followed. In tests, noise at the 3.3-V output was about 5 mV p-p at the 150-kHz switcher

frequency. Note that the LDO noise rejection for such relatively high frequencies is much less than at 100/120 Hz. Note also that C2's ESR will indirectly control the final noise output. The ripple figures given are for a general-purpose C2 part, and can be improved.

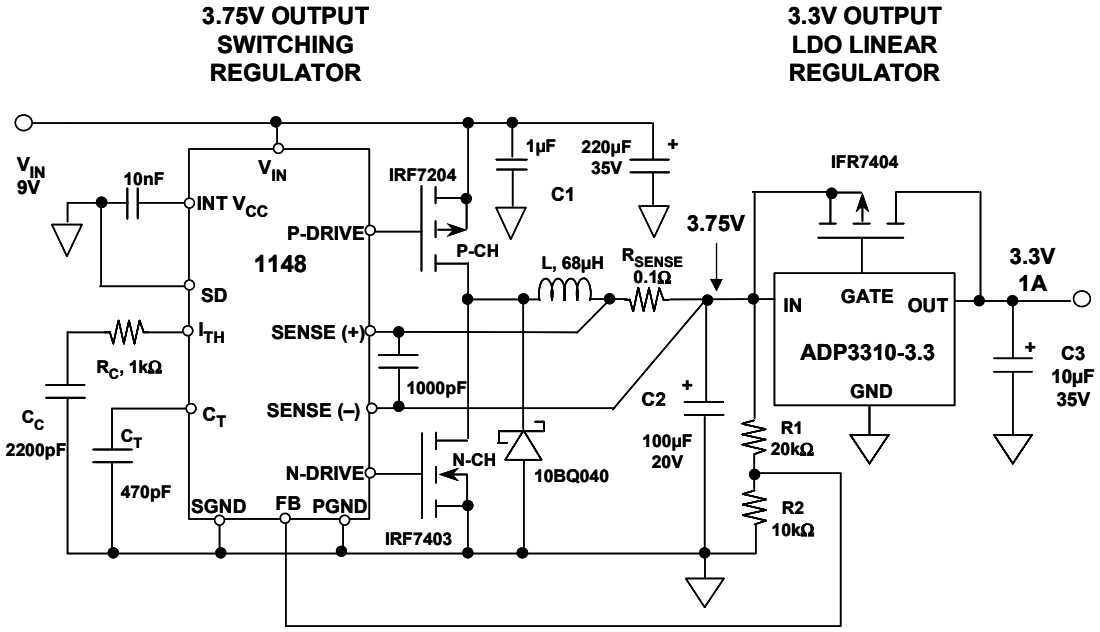


Figure 9.62: *A Linear Post-Regulator Operating After a Switching/Linear Regulator is Capable of Low Noise, as Well as Good DC Efficiency*

Grounding Linear and Switching Regulators

The importance of maintaining a low impedance large area ground plane is critical to practically all analog circuits today, especially high current low dropout linear regulators or switching regulators. The ground plane not only acts as a low impedance return path for high frequency switching currents but also minimizes EMI/RFI emissions. In addition, it serves to minimize unwanted voltage drops due to high load currents. Because of the shielding action of the ground plane, the circuit's susceptibility to external EMI/RFI is also reduced. When using multilayer PC boards, it is wise to add a power plane. In this way, low impedances can be maintained on both critical layers.

Figure 9.63 shows a grounding arrangement for a low dropout linear regulator such as the ADP3310. It is important to minimize the total voltage drop between the input voltage and the load, as this drop will subtract from the voltage dropped across the pass transistor and reduce its headroom. For this reason, these runs should be wide, heavy traces and are indicated by the wide interconnection lines on the diagram. The low-current ground (GND) and V_{OUT} (sense) pins of the ADP3310 are connected directly to the load so that the regulator regulates the voltage at the load rather than at its own output. The IS and V_{IN} connections to the R_S current sense resistor should be made directly to the resistor terminals to minimize parasitic resistance, since the current limit resistor is typically a very low value (milliohms). In fact, for very low values it may actually consist of a PC board trace of the proper width, length, and thickness to yield the desired resistance.

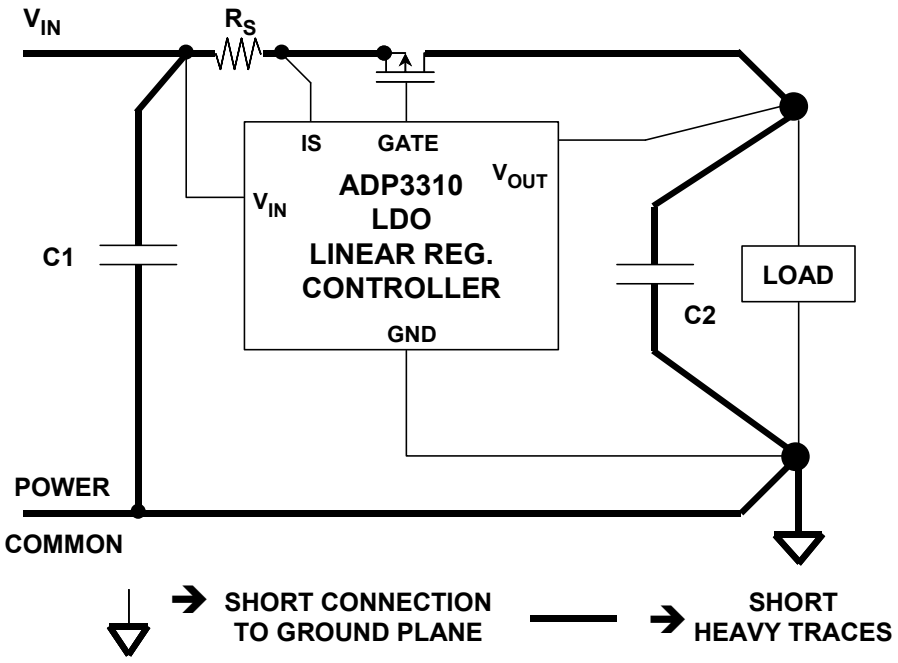


Figure 9.63: *Grounding and Signal Routing Techniques for Low Dropout Regulators Method 1*

The input decoupling capacitor (C1) should be connected with short leads at the regulator input in order to absorb any transients which may couple onto the input voltage line. Similarly, the load capacitor (C2) should have minimum lead length in order to absorb transients at that point and prevent them from coupling back into the regulator. The single-point connection to the low impedance ground plane is made directly at the load.

Figure 9.64 shows a grounding arrangement which is similar to that of Figure 9.63 with the exception that all ground connections are made with direct connections to the ground plane. This method works extremely well when the regulator and the load are on the same PC board, and the load is distributed around the board rather than located at one specific point. If the load is not distributed, the connection from V_{OUT} (sense) should be connected directly to the load as shown by the dotted line in the diagram. This ensures the regulator provides the proper voltage at the load regardless of the drop in the trace connecting the pass transistor output to the load.

Switching regulators present major challenges with respect to layout, grounding, and filtering. The discussion above on linear regulators applies equally to switchers, although the importance of dc voltage drops may not be as great.

There is no way to eliminate high frequency switching currents in a switching regulator, since they are necessary for the proper operation of the regulator. What one must do, however, is to recognize the high switching current paths and take proper measures to ensure that they do not corrupt circuits on other parts of the board or system. Figure 9.65 shows a generic synchronous switching regulator controller IC and the associated external MOSFET switching transistors. The heavy bold lines indicate the paths where

there are large switching currents and/or high dc currents. Notice that all these paths are connected together at a single-point ground which in turn connects to a large area ground plane.

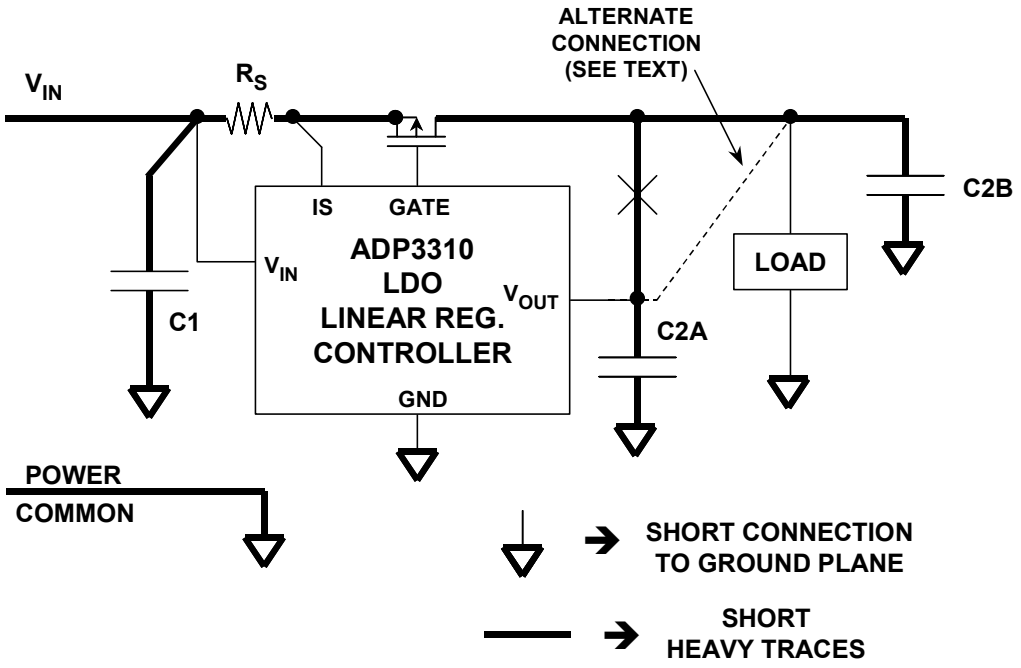


Figure 9.64: *Grounding and Signal Routing for Low Dropout Regulator Method 2*

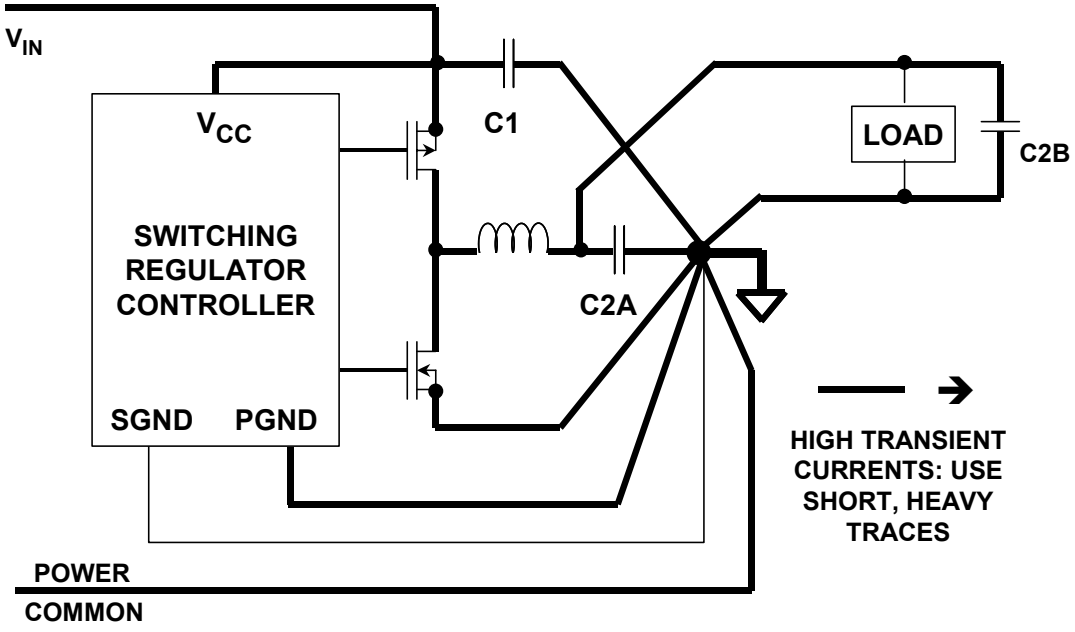


Figure 9.65: *Grounding and Signal Routing Techniques for Switching Regulators Method 1*

In order to minimize stray inductance and resistance, each of the high current paths should be as short as possible. Capacitors C1 and C2A must absorb the bulk of the input and output switching current and shunt it to the single-point ground. Any additional resistance or inductance in series with these capacitors will degrade their effectiveness. Minimizing the area of all the loops containing the switching currents prevents them from significantly affecting other parts of the circuit. In actual practice, however, the single-point concept in Figure 9.65 is difficult to implement without adding additional lead length in series with the various components. The added lead length required to implement the single-point grounding scheme tends to degrade the effects of using the single-point ground in the first place.

A more practical solution is to make multiple connections to the ground plane and make each of them as short as possible. This leads to the arrangement shown in Figure 9.66, where each critical ground connection is made directly to the ground plane with the shortest connection length possible. By physically locating all critical components associated with the regulator close together and making the ground connections short, stray series inductance and resistance are minimized. It is true that several small ground loops may occur using this approach, but they should not cause significant system problems because they are confined to a very small area of the overall large-area ground plane.

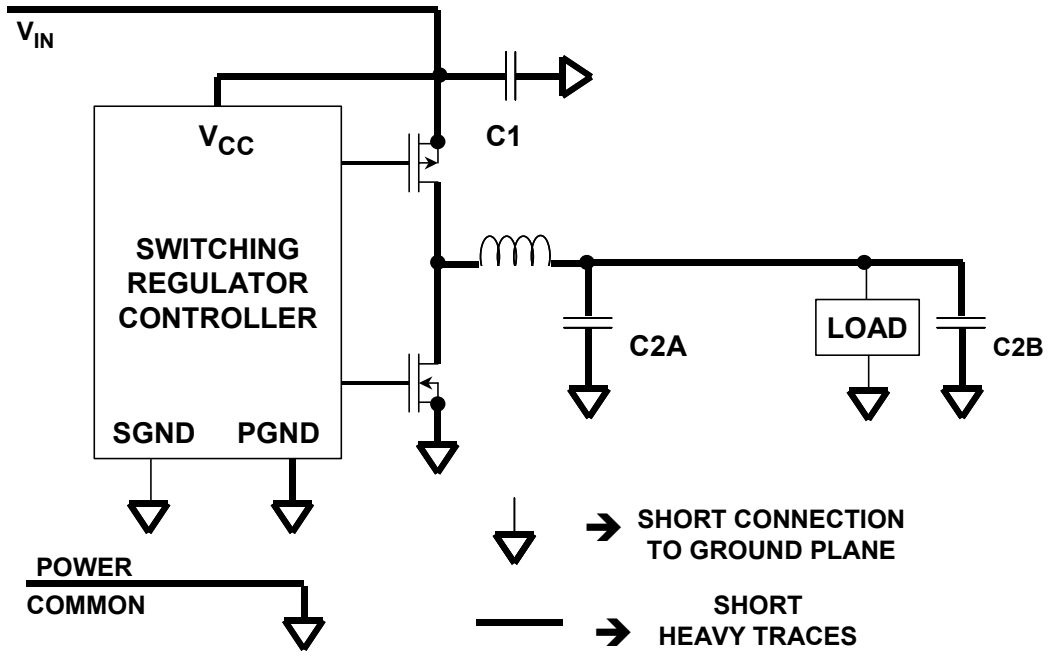


Figure 9.66: *Grounding and Signal Routing Techniques for Switching Regulators Method 2*

Power Supply Noise Reduction and Filtering

During the last decade or so, switching power supplies have become much more common in electronic systems. As a consequence, they also are being used for analog supplies. Good reasons for the general popularity include their high efficiency, low temperature rise, small size, and light weight, as opposed to equivalent-power linear regulators.

In spite of these benefits, switchers *do* have drawbacks, most notably high output noise. This noise generally extends over a broad band of frequencies, resulting in both conducted and radiated noise, as well as unwanted electric and magnetic fields. Voltage output noise of switching supplies are short-duration voltage transients, or spikes. Although the fundamental switching frequency can range from 20 kHz to 1 MHz, the spikes can contain frequency components extending to 100 MHz or more. While specifying switching supplies in terms of rms noise is common vendor practice, as a user you should also specify the *peak* (or peak-to-peak) amplitudes of the switching spikes, with the output loading of your system.

This section discusses filter techniques for rendering a switching regulator output *analog ready*, that is sufficiently quiet to power precision op amp and other analog circuitry with relatively small loss of dc terminal voltage. The filter solutions presented are generally applicable to all power supply types incorporating switching element(s) in their energy path. This includes charge-pump as well as other switching type converters and supplies. This section focuses on reducing *conducted type* switching power supply noise with external post filters, as opposed to radiated type noise.

Tools useful for combating high frequency switcher noise are shown by Figure 9.67. These differ in electrical characteristics as well as practicality towards noise reduction, and are listed roughly in an order of priorities. Of these tools, L and C are the most powerful filter elements, and are the most cost-effective, as well as small in size.

- **Capacitors**
- **Inductors**
- **Ferrites**
- **Resistors**
- **Linear Post Regulation**
- **Proper Layout and Grounding**
- **Physical Separation!**

Figure 9.67: *Tools Useful in Reducing Power Supply Noise*

Capacitors

Capacitors are probably the single most important filter component for reducing switching-related noise. As noted in the first section of this chapter, there are many different types of capacitors. It is also quite true that understanding of their individual characteristics is absolutely mandatory to the design of effective and practical power supply filters. There are generally three classes of capacitors useful in 10-kHz to 100-MHz filters, broadly distinguished as the generic dielectric types; *electrolytic*, *film*, and *ceramic*. These discussions complement earlier ones, focusing on power-related concepts.

With any dielectric, a major potential filter loss element is ESR (equivalent series resistance), the net parasitic resistance of the capacitor. ESR provides an ultimate limit to

filter performance, and requires more than casual consideration, because it can vary both with frequency and temperature in some types. Another capacitor loss element is ESL (equivalent series inductance). ESL determines the frequency where the net impedance characteristic switches from capacitive to inductive. This varies from as low as 10 kHz in some electrolytics to as high as 100 MHz or more in chip ceramic types. Both ESR and ESL are reduced when a leadless package is used. All capacitor types mentioned are available in surface mount packages, preferable for high speed uses.

The *electrolytic* family provides an excellent, cost-effective low-frequency filter component, because of the wide range of values, a high capacitance-to-volume ratio, and a broad range of working voltages. It includes *general purpose aluminum electrolytic* types, available in working voltages from below 10 V up to about 500 V, and in size from 1 to several thousand μF (with proportional case sizes). All electrolytic capacitors are polarized, and cannot withstand more than a volt or so of reverse bias without damage.

A subset of the general electrolytic family includes *tantalum* types, generally limited to voltages of 100 V or less, with capacitance of 500 μF or less (see Reference 7). In a given size, tantalums exhibit a higher capacitance-to-volume ratios than do general purpose electrolytics, and have both a higher frequency range and lower ESR. They are generally more expensive than standard electrolytics, and must be carefully applied with respect to surge and ripple currents.

A subset of aluminum electrolytic capacitors is the *switching* type, designed for handling high pulse currents at frequencies up to several hundred kHz with low losses (see Reference 8). This capacitor type can compete with tantalums in high frequency filtering applications, with the advantage of a broader range of values.

A more specialized high performance aluminum electrolytic capacitor type uses an organic semiconductor electrolyte (see Reference 9). The *OS-CON* capacitors feature appreciably lower ESR and higher frequency range than do other electrolytic types, with an additional feature of minimal low-temperature ESR degradation.

Film capacitors are available in very broad value ranges and an array of dielectrics, including polyester, polycarbonate, polypropylene, and polystyrene. Because of the low dielectric constant of these films, their volumetric efficiency is quite low, and a 10-μF/50-V polyester capacitor (for example) is actually a handful. Metalized (as opposed to foil) electrodes does help to reduce size, but even the highest dielectric constant units among film types (polyester, polycarbonate) are still larger than any electrolytic, even using the thinnest films with the lowest voltage ratings (50 V). Where film types excel is in their low dielectric losses, a factor which may not necessarily be a practical advantage for filtering switchers. For example, ESR in film capacitors can be as low as 10 mΩ or less, and the behavior of films generally is very high in terms of Q. In fact, this can cause problems of spurious resonance in filters, requiring damping components.

As typically constructed using wound layers, film capacitors can be inductive, which limits their effectiveness for high frequency filtering. Obviously, only non-inductively made film caps are useful for switching regulator filters. One specific style which is non-inductive is the *stacked-film* type, where the capacitor plates are cut as small overlapping

linear sheet sections from a much larger wound drum of dielectric/plate material. This technique offers the low inductance attractiveness of a plate sheet style capacitor with conventional leads (see References 8 and 10). Obviously, minimal lead length should be used for best high frequency effectiveness. Very high current polycarbonate film types are also available, specifically designed for switching power supplies, with a variety of low inductance terminations to minimize ESL (see Reference 11). Dependent upon their electrical and physical size, film capacitors can be useful at frequencies to above 10 MHz. At the highest frequencies, only stacked film types should be considered. Leadless surface mount packages are now available for film types, minimizing inductance.

Ceramic is often the capacitor material of choice above a few MHz, due to its compact size, low loss, and availability up to several μF in the high-K dielectric formulations (X7R and Z5U), at voltage ratings up to 200 V (see ceramic families of Reference 7).

Multilayer ceramic "chip caps" are very popular for bypassing and/or filtering at 10 MHz or more, simply because their very low inductance design allows near optimum RF bypassing. For smaller values, ceramic chip caps have an operating frequency range to 1 GHz. For high frequency applications, a useful selection can be ensured by selecting a value which has a self-resonant frequency *above* the highest frequency of interest.

The capacitor model and waveforms of Figure 9.68 illustrate how the various parasitic model elements become dominant, dependent upon the operating frequency. Assume an input current pulse changing from 0 to 1 A in 100 ns, as noted in the figure, and consider what voltage will be developed across the capacitor.

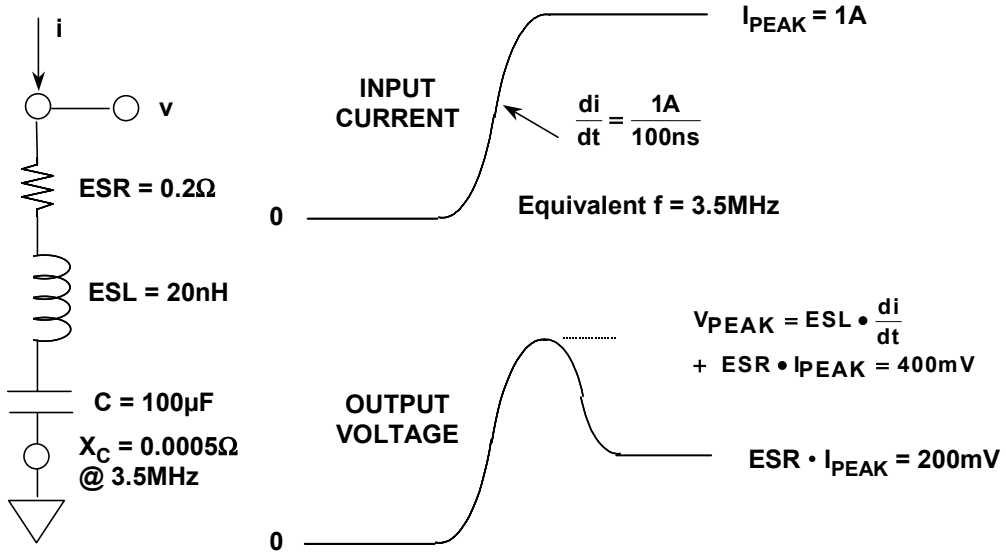


Figure 9.68: *Capacitor Equivalent Circuit and Response to Input Current Pulse*

The fast-rising edge of the current waveform shown results in an initial voltage peak across the capacitor, which is proportional to the ESL. After the initial transient, the voltage settles down to a longer duration level which is proportional to the ESR of the capacitor. Thus the ESL determines how effective a filter the capacitor is for the fastest

components of the current signal, and the ESR is important for longer time frame components. Note that an overall time frame of a few microseconds (or even less) is relevant here. As things turn out, this means switching frequencies in the 100-kHz to 1-MHz range. Unfortunately however, this happens to be the region where most electrolytic types begin to perform poorly.

All electrolytics will display impedance curves similar in general shape to that of Figure 9.69. In a practical capacitor, at frequencies below about 10 kHz the net impedance seen at the terminals is almost purely capacitive (C region). At intermediate frequencies, the net impedance is determined by ESR, for example about 0.1 to 0.5 Ω at ~125 kHz, for several types (ESR region). Above about several hundred kHz to 1 MHz these capacitor types become inductive, with net impedance rising (ESL region).

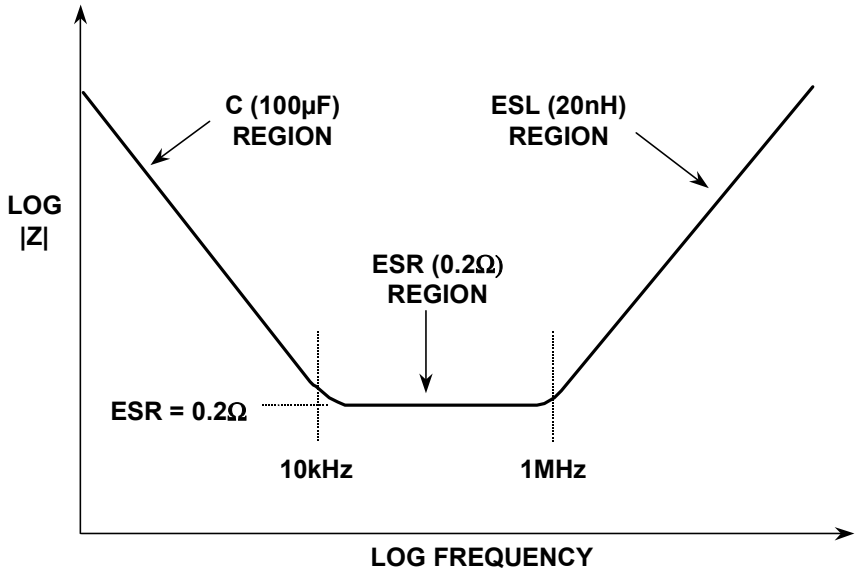


Figure 9.69: *Electrolytic Capacitor Impedance Versus Frequency*

The minimum impedance within the 10 kHz to 1 MHz range will vary with the magnitude of the capacitor's ESR. This is the primary reason why ESR is the most critical item in determining a given capacitor's effectiveness as a switching supply filter element. Higher up in frequency, the inductive region will vary with ESL (which in turn is also strongly effected by package style). It should go without saying that a wideband impedance plot for a capacitor being considered for a filter application will go a long way towards predicting its potential value, as well as for comparing one type against another.

It should be understood that all real world capacitors have some finite ESR. While it is usually desirable for filter capacitors to possess low ESR, this isn't always so. In some cases, the ESR may actually be helpful in reducing resonance peaks in filters, by supplying "free" damping. For example, in most electrolytic types, a nominally flat broad series resonance region can be noted in an impedance vs. frequency plot. This occurs where |Z| falls to a minimum level, nominally equal to the capacitor's ESR at that frequency. This low Q resonance can generally be noted to cover a relatively wide frequency range of several octaves. Contrasted to the high Q sharp resonances of film and ceramic caps, electrolytic's low Q behavior can be useful in controlling resonant peaks.

Ferrites

A second important filter element is the inductor, available in various forms. The use of *ferrite* core materials is prevalent in inductors most practical for power supply filtering.

Regarding inductors, ferrites, which are non-conductive ceramics manufactured from the oxides of nickel, zinc, manganese, etc., are extremely useful in power supply filters (see Reference 12). Ferrites can act as either inductors or resistors, dependent upon their construction and the frequency range. At low frequencies (<100 kHz), inductive ferrites are useful in low-pass LC filters. At higher frequencies, ferrites become resistive, which can be an important characteristic in high-frequency filters. Again, exact behavior is a function of the specifics. Ferrite impedance depends on material, operating frequency range, dc bias current, number of turns, size, shape, and temperature. Figure 9.70 summarizes a number of ferrite characteristics.

- **Ferrites Good for Frequencies Above 25kHz**
- **Many Sizes / Shapes Available Including Leaded "Resistor Style"**
- **Ferrite Impedance at High Frequencies Primarily Resistive -- Ideal for HF Filtering**
- **Low DC Loss: Resistance of Wire Passing Through Ferrite is Very Low**
- **High Saturation Current Versions Available**
- **Choice Depends Upon:**
  - **Source and Frequency of Interference**
  - **Impedance Required at Interference Frequency**
  - **Environmental: Temperature, AC and DC Field Strength, Size and Space Available**
- **Always Test the Design!**

Figure 9.70: *A Summary of Ferrite Characteristics*

Several ferrite manufacturers offer a wide selection of ferrite materials from which to choose, as well as a variety of packaging styles for the finished network (see References 13 and 14). A simple form is the *bead* of ferrite material, a cylinder of the ferrite which is simply slipped over the power supply lead to the decoupled stage. Alternately, the *leaded ferrite bead* is the same bead, pre-mounted on a length of wire and used as a component (see Reference 14). More complex beads offer multiple holes through the cylinder for increased decoupling, plus other variations. Surface mount beads are also available. PSpice models of Fair-Rite ferrites are available, allowing ferrite impedance estimations (see Reference 15). The models match measured rather than theoretical impedances.

A ferrite's impedance is dependent upon a number of inter-dependent variables, and is difficult to quantify analytically, thus selecting the proper ferrite is not straightforward. However, knowing the following system characteristics will make selection easier. First, determine the frequency range of the noise to be filtered. Second, the expected temperature range of the filter should be known, as ferrite impedance varies with temperature. Third, the dc current flowing through the ferrite must be known, to ensure that the ferrite does not saturate. Although models and other analytical tools may prove

useful, the general guidelines given above, coupled with actual filter experimentation connected under system load conditions, should lead to a proper ferrite selection.

Card Entry Filter

Using proper component selection, low and high frequency band filters can be designed to smooth a noisy switching supply output so as to produce an *analog ready* supply. It is most practical to do this over two (and sometimes more) stages, each stage optimized for a range of frequencies.

A basic stage can be used to carry the entire load current, and filter noise by 60 dB or more up to a 1- to 10-MHz range. Figure 9.71 illustrates this type of filter, which is used as a *card entry filter,* providing broadband filtering for all power entering a PC card.

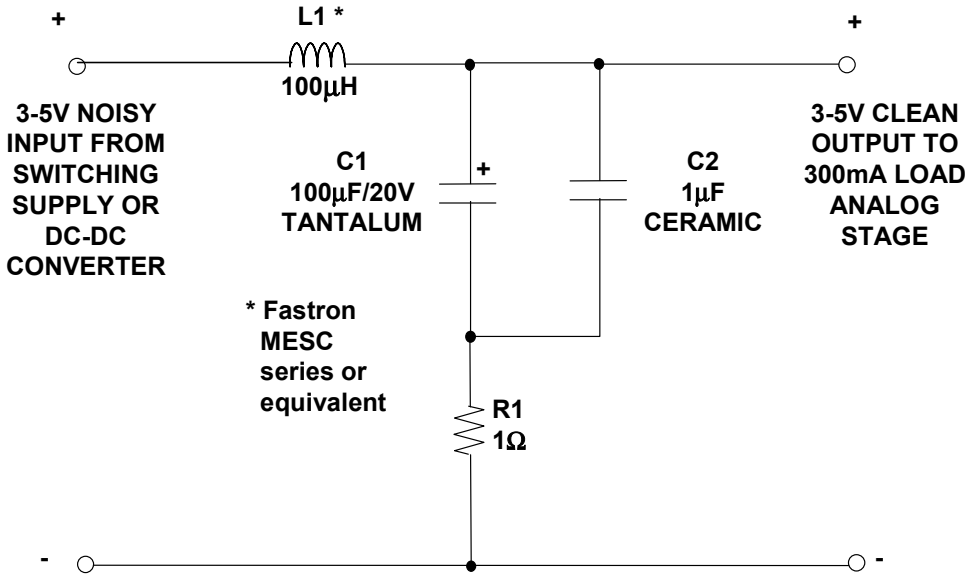


Figure 9.71: *A Card-Entry Filter is Useful for Low-Medium Frequency Power Line Noise Filtering in Analog Systems*

In this filter, L1 and C1 perform the primary filtering, which provides a corner frequency of about 1.6 kHz. With the corner thus placed well below typical switching frequencies, the circuit can have good attenuation up to 1 MHz, where the typical attenuation is on the order of 60 dB. At higher frequencies parasitics limit performance, and a second filter stage will be more useful.

The ultimate level of performance available from this filter will be related to the components used within it. L1 should be derated for the operating current, thus for 300-mA loads it is a 1-A type. The specified L1 choke has a typical dc resistance of 0.65 Ω, for low drop across the filter (see Reference 16). C1 can be either a tantalum or an aluminum electrolytic, with moderately low ESR. For current levels lower than 300 mA, L1 can be proportionally downsized, saving space. The resistor R1 provides damping for the LC filter, to prevent possible ringing. R1 can be reduced or even possibly eliminated, if the ESR of C1 provides a comparable impedance.

While the example shown is a single-supply configuration, obviously the same filter concepts apply for dual supplies.

Rail Bypass/Distribution Filter

A complement to the card-entry filter is the rail-bypass filter scheme of Figure 9.72. When operating from relatively clean power supplies, the heavy noise filtering of the card entry filter may not be necessary. However, some sort of low frequency bypassing with appreciable energy storage is almost always good, and this is especially true if high currents are being delivered by the stages under power.

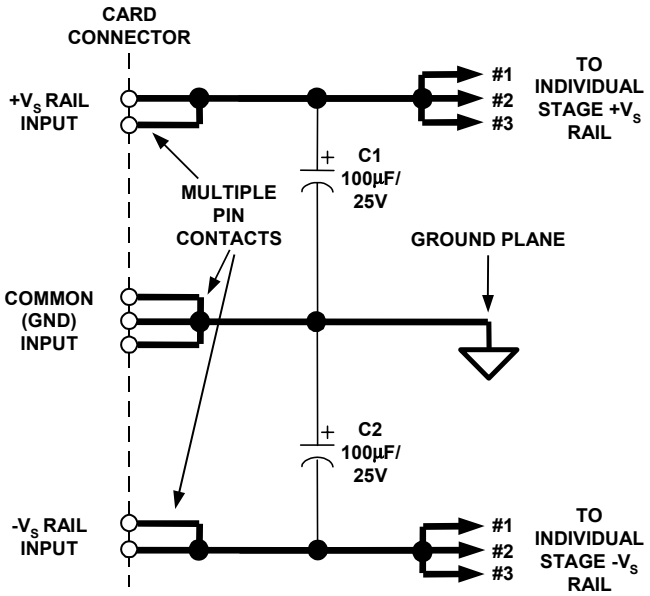


Figure 9.72: *Dual-Supply Low Frequency Rail Bypass/Distribution Filter*

In such cases, some lumped low frequency bypassing is appropriate on the card. Although these energy storage filters need not be immediately adjacent to the ICs they serve, they should be within a few inches. This type of bypassing scheme should be considered a minimum for powering any analog circuit. The exact capacitor values aren't critical, and can vary appreciably. The most important thing is to avoid leaving them out! The circuit shown uses C1 and C2 as these bypasses in a dual-rail system. Note that multiple card contacts are recommended for the I/O pins, especially ground connection. From the capacitors outward, supply rail traces are distributed to each stage as shown, in "star" distribution fashion. Note—while this is the optimum method to minimize inter-stage crosstalk, in practice some degree of "daisy chaining" is often difficult to avoid. A prudent designer should therefore carefully consider common supply currents effects in designing these PCB distribution paths.

Wider than normal traces are recommended for these supply rails, especially those carrying appreciable current. If the current levels are in the ampere region, then star-type supply distribution with ultra-wide traces should be considered mandatory. In extreme cases, a dedicated power plane can be used. The impedance of the ground return path is minimized by the use of a ground plane.

Local High Frequency Bypass/Decoupling

At each individual analog stage, further local, high-frequency-only filtering is used. With this technique, used in conjunction with either the card-entry filter or the low frequency bypassing network, such smaller and simpler local filter stages provide optimum high frequency decoupling. *These stages are provided directly at the power pins, of* all *individual analog stages*.

Figure 9.73 shows this technique, in both correct (left) as well as incorrect example implementations (right). In the left example, a typical 0.1-µF chip ceramic capacitor goes directly to the opposite PCB side ground plane, by virtue of the via, and on to the IC's GND pin by a second via. In contrast, the less desirable setup at the right adds additional PCB trace inductance in the ground path of the decoupling cap, reducing effectiveness.

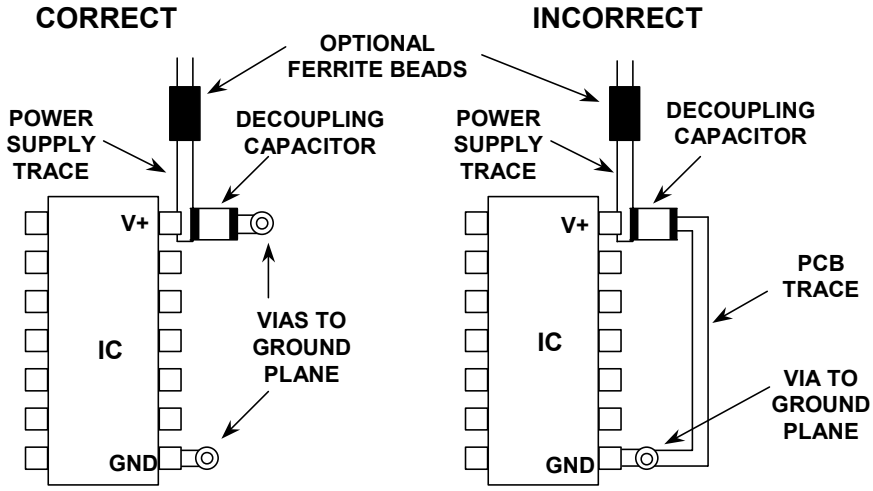


Figure 9.73: *Localized High Frequency Supply Filter(S) Provides Optimum Filtering and Decoupling Via Short Low-Inductance Path (Ground Plane)*

The general technique is shown here as suitable for a single-rail power supply, but the concept obviously extends to dual rail systems. Note—if the decoupled IC in question is an op amp, the GND pin shown is the $-V_S$ pin. For dual supply op amp uses, there is no op amp GND pin per se, so the dual decoupling networks should go directly to the ground plane when used, or other local ground.

All high frequency (i.e., ≥10 MHz) ICs should use a bypassing scheme similar to Figure 9.73 for best performance. Trying to operate op amps and other high performance ICs without local bypassing is almost always folly. It *may* be possible in a few circumstances, *if* the circuitry is strictly micropower in nature, and the gain-bandwidth in the kHz range. To put things into an overall perspective however, note that a pair of 0.1-µF ceramic bypass caps cost less than 25 cents. Hardly a worthy saving compared to the potential grief and lost time of troubleshooting a system without bypassing!

In contrast, the ferrite beads aren't 100% necessary, but they will add extra high frequency noise isolation and decoupling, which is often desirable. Possible caveats here

would be to verify that the beads never saturate, when the op amps are handling high currents.

Note that with some ferrites, even before full saturation occurs, some beads can be non-linear, so if a power stage is required to operate with a low distortion output, this should also be lab checked.

Figure 9.74 summarizes the previous points of this section regarding power supply conditioning techniques for high performance analog circuitry.

- **Use Proper Layout and Grounding Techniques!**
- **At HF Local Decoupling at IC Power Pins is Mandatory**
- **At HF Ground Planes are Mandatory**
- **External LC Filters Very Effective in Reducing Ripple**
- **Low ESR/ESL Capacitors Give Best Results**
- **Parallel Caps Lower ESR/ESL and Increase C**
- **Linear Post Regulation Effective for Noise Reduction and Best Regulation**
- **Completely Analytical Approach Difficult**
  -- Prototyping Required for Optimum Results
- **Once Design is Final, Don't Switch Vendors or Substitute Parts**
  -- Without First Verifying Performance Within the Circuit!

Figure 9.74: *A Summary of Power Supply Conditioning Techniques for High Performance Analog Circuitry*

REFERENCES:
9.3 ANALOG POWER SUPPLY SYSTEMS

1. Walt Jung, "References and Low Dropout Linear Regulators," Section 2 within Walt Kester, Ed., **Practical Design Techniques for Power and Thermal Management**, Analog Devices, Inc., 1998, ISBN 0-916550-19-2.

2. Paul Brokaw, "A Simple Three-Terminal IC Bandgap Voltage Reference," **IEEE Journal of Solid State Circuits**, Vol. SC-9, December, 1974.

3. Frank Goodenough, "Vertical-PNP-Based Monolithic LDO Regulator Sports Advanced Features," **Electronic Design**, May 13, 1996.

4. Frank Goodenough, "Low Dropout Regulators Get Application Specific," **Electronic Design**, May 13, 1996.

5. Walt Kester, Brian Erisman, Gurgit Thandi, "Switched Capacitor Voltage Converters," Section 4 within Walt Kester, Editor, **Practical Design Techniques for Power and Thermal Management**, Analog Devices, Inc., 1998, ISBN 0-916550-19-2.

6. Walt Jung, Walt Kester, Bill Chesnut, "Power Supply Noise Reduction and Filtering," portion of Section 8 within Walt Kester, Editor, **Practical Design Techniques for Power and Thermal Management**, Analog Devices, Inc., 1998, ISBN 0-916550-19-2.

7. **Tantalum Electrolytic and Ceramic Capacitor Families**, Kemet Electronics, Box 5928, Greenville, SC, 29606, (803) 963-6300.

8. Type HFQ Aluminum Electrolytic Capacitor and Type V Stacked Polyester Film Capacitor, Panasonic, 2 Panasonic Way, Secaucus, NJ, 07094, (201) 348-7000.

9. **OS-CON Aluminum Electrolytic Capacitor Technical Book**, Sanyo, 3333 Sanyo Road, Forrest City, AK, 72335, (501) 633-6634.

10. Ian Clelland, "Metallized Polyester Film Capacitor Fills High Frequency Switcher Needs," **PCIM**, June 1992.

11. Type 5MC Metallized Polycarbonate Capacitor, Electronic Concepts, Inc., Box 1278, Eatontown, NJ, 07724, (908) 542-7880.

12. Henry W. Ott, **Noise Reduction Techniques in Electronic Systems, 2nd Edition**, John Wiley, Inc., 1988, ISBN: 0-471-85068-3.

13. **Fair-Rite Linear Ferrites Catalog**, Fair-Rite Products, Box J, Wallkill, NY, 12886, (914) 895-2055.

14. Type EXCEL leaded ferrite bead EMI filter, and Type EXC L leadless ferrite bead, Panasonic, 2 Panasonic Way, Secaucus, NJ, 07094, (201) 348-7000.

15. Steve Hageman, "Use Ferrite Bead Models to Analyze EMI Suppression," **The Design Center Source,** MicroSim Newsletter**,** January, 1995.

16. "MESC series RFI suppression chokes," FASTRON GmbH, Zum Kaiserblick 25, 83620 Feldkirchen-Westerham, Germany, www.fastron.de

NOTES:

SECTION 9.4: OVERVOLTAGE PROTECTION

Walt Jung, Walt Kester, James Bryant, Joe Buxton, Wes Freeman

Frequently, data converters, op amps, and other analog ICs require protection against destructive potentials at their input and output terminals. One basic reason behind this is that these ICs are by nature relatively fragile components. Although designed to be as robust as possible *for normal signals*, there are nevertheless certain application and/or handling conditions where they can see voltage transients beyond their ratings. This situation can occur for either of two instances. The first of these is *in-circuit,* that is, operating within an application circuit. The second instance is *out-of-circuit,* which might be at anytime after receipt from a supplier, but prior to final assembly and mounting of the IC. In either case, under overvoltage conditions, it is a basic fact-of-life that unless the designer limits the fault currents at the input (or possibly output) of the IC, it can be damaged or destroyed.

So, obviously the designer should fully understand all of the fault mechanisms internal to those ICs that may require protection. This then allows design of networks that can protect the in-circuit IC throughout its lifetime, without undue compromise of speed, precision, etc. Or, for the out-of-circuit IC, it can help define proper protective handling procedures until it reaches its final destination. This section of the chapter examines a variety of protection schemes to ensure adequate protection for op amps and other analog ICs for in-circuit applications, as well as for out-of-circuit environments.

In-Circuit Overvoltage Protection

There are many common cases that stress op amps and other analog ICs at the input, while operating within an application, i.e., in-circuit. Since these ICs must often interface to the outside world, this may entail handling voltages exceeding their absolute maximum ratings. For example, sensors are often placed in environments where a fault condition can expose the circuit to a dangerously high voltage. With the sensor connected to a signal processing amplifier, the input then sees excessive voltages during a fault.

General Input Common Mode Limitations

Whenever the op amp or data converter input common-mode (CM) voltage goes outside its supply range, the device can be damaged, even if the supplies are turned off. Accordingly, the absolute maximum input ratings of almost all linear ICs limits the greatest applied voltage to a level equal to the positive and negative supply voltage, plus about 0.3 V beyond these voltages (i.e., $+V_S$ + 0.3 V, or $–V_S$ – 0.3 V). While some exceptions to this general rule might exist it is important to note this: *Most linear ICs require input protection when overvoltage of more than 0.3 V beyond the rails occurs.*

A safe operating rule is to always keep the applied CM voltage between the rail limits. Here, "safe" implies prevention of outright IC destruction. As will be seen later, there are also intermediate "danger-zone" CM conditions between the rails with certain devices, which can invoke dangerous (but not necessarily destructive) behavior.

Speaking generally, it is important to note that almost *any* op amp or data converter input will break down, given sufficient overvoltage to the positive or negative rail. Under breakdown conditions high and uncontrolled current can flow, so the danger is obvious. The exact breakdown voltage is entirely dependent on the individual op amp input stage. It may be a 0.6-V diode drop, or a process-related breakdown of 50 V or more. In many cases, overvoltage stress can result in currents over 100 mA, which destroys a part almost instantly.

Therefore, unless otherwise stated on the data sheet, input fault current should be limited to ≤5 mA to avoid damage. This is a conservative guideline, based on metal trace widths in a typical op amp or data converter input. Higher levels of current can cause *metal migration*, a cumulative effect, which, if sustained, eventually leads to an open trace. Should a migration situation be present, failure may only appear after a long time due to multiple overvoltages, a very difficult failure to identify. So, even though an amplifier may appear to withstand overvoltage currents well above 5 mA for a short time period, it is important to limit the current to 5 mA (or preferably less) for long term reliability.

Figure 9.75 illustrates an external, general-purpose op amp CM protection circuit. The basis of this scheme is the use of Schottky diodes D1 and D2, plus an external current limiting resistor, R_{LIMIT}. With appropriate selection of these parts, input protection for a great many op amps can be ensured. Note that an op amp may also have *internal* protection diodes to the supplies (as shown) which conduct at about 0.6-V forward drop above or below the respective rails. In this case however, the external Schottky diodes effectively parallel any internal diodes, so the internal units never reach their threshold. Diverting fault currents externally eliminates potential stress, protecting the op amp.

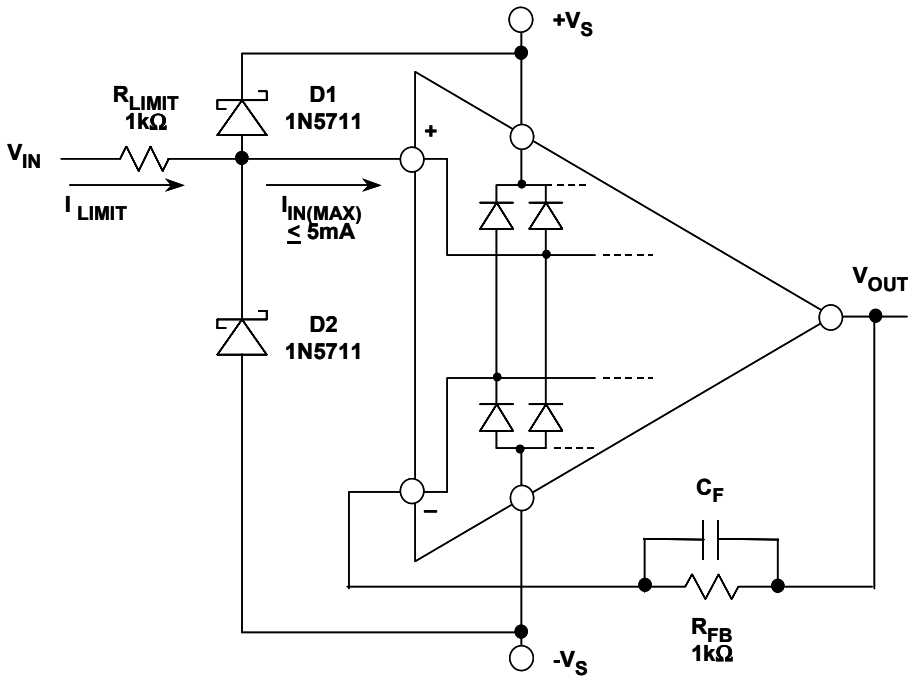


Figure 9.75: *A General-Purpose Op Amp CM Overvoltage Protection Network Using Schottky Clamp Diodes with Current Limit Resistance*

The external diodes also allow other degrees of freedom, some not so obvious. For example, if fault current is allowed to flow in the op amp, R_{LIMIT} must then be chosen so that the maximum current is no more than 5 mA for the worst case V_{IN}. This criterion can result in rather large R_{LIMIT} values, and the associated increase in noise and offset voltage may not be acceptable. For instance, to protect against a V_{IN} of 100 V with the 5-mA criterion, R_{LIMIT} must be ≥20 kΩ. However with external Schottky clamping diodes, this allows R_{LIMIT} to be governed by the maximum allowable D1-D2 current, which can be larger than 5 mA. However, care must be used here, for at very high currents the Schottky diode drop may exceed 0.6 V, possibly activating internal op amp diodes.

It is very useful to keep the R_{LIMIT} value as low as possible, to minimize offset and noise errors. R_{LIMIT}, in series with the op amp input, produces a bias-current-proportional voltage drop. Left uncorrected, this voltage appears as an increase in the circuit's offset voltage. Thus for op amps where the bias currents are moderate and approximately equal (most bipolar types) compensation resistor R_{FB} balances the dc effect, and minimizes this error. For low bias current op amps (I_b ≤10 nA, or FET types) it is likely R_{FB} won't be necessary. To minimize noise associated with R_{FB}, bypass it with a capacitor, C_F.

Clamping Diode Leakage

For obvious reasons, it is critical that diodes used for protective clamping at an op amp input have a leakage sufficiently low to not interfere with the bias level of the application. Figure 9.76 illustrates how some well-known diodes differ in terms of leakage current, as a function of the reverse bias voltage, Vbias.

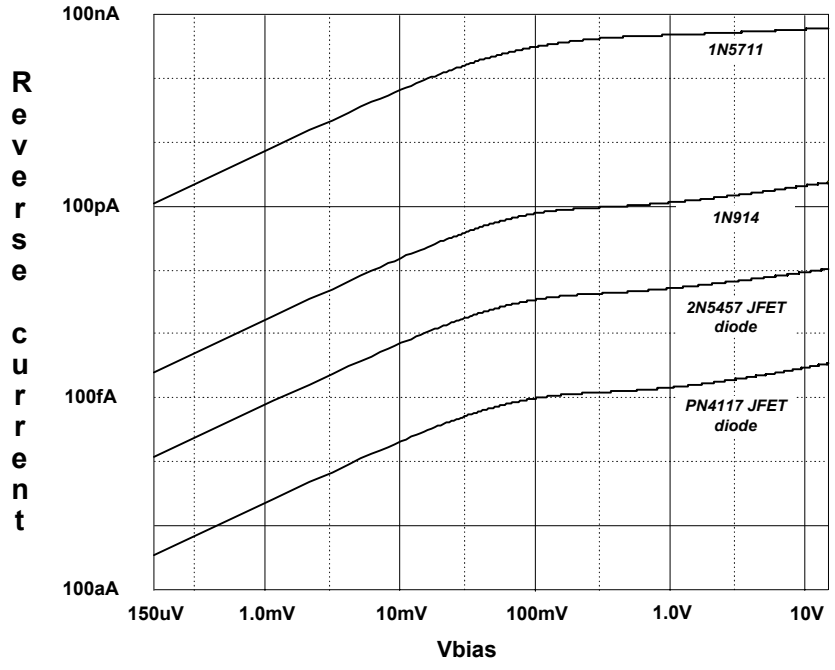


Figure 9.76: *Reverse Bias Current Characteristics for Diodes Useful in Protective Clamping Networks (PSpice Simulation)*

In this chart, a 25°C simulation using PSpice diode models, it is easy to see that not only is the diode type critical, so is the reverse bias. The 1N5711 Schottky type for example, has a leakage of nearly 100 nA at a reverse bias of 15 V, as it would typically be used with a ±15-V powered op amp. With this level of leakage, such diodes will only be useful with op amps with bias currents of several μA. For protection of appreciably lower bias current op amps (particularly most FET input devices) much lower leakage is necessary.

As the data of Figure 9.76 shows, not only does selecting a better diode help control leakage current, but operating it at a low bias voltage condition reduces leakage substantially. For example, while an ordinary 1N914 or 1N4148 diode may have 200-pA of leakage at 15 V, this is reduced to slightly more than 1 pA with bias controlled to 1 mV. But there is a caveat here! When used in a high impedance clamp circuit, glass diodes such as the 1N914/1N4148 families should either be shielded from incident light, or use opaque packages. This is necessary to minimize parasitic photocurrent from the surrounding light, which effectively appears as diode leakage current.

Specialty diodes with much lower leakage are also available, such as diode-connected FET devices characterized as protection diodes (see DPAD series of Reference 2). Within the data of Figure 9.76, the 2N5457 is a general purpose JFET, and the 2N4117/PN4117 family consists of parts designed for low current levels. Other low leakage and specialty diodes are described in References 3 and 4.

Finally, whenever protective diodes are used, the effects of their capacitance on circuit performance must be analyzed.

A Flexible Voltage Follower Protection Circuit

Of course, it isn't a simple matter to effectively apply protective clamping to op amp inputs, while reducing diode bias level to a sub-mV level.

The circuit of Figure 9.77 shows low-leakage input clamping and other means used with a follower connected FET op amp, with protection at input and output, for both power on or off conditions.

Disregarding the various diodes momentarily, this circuit is an output-current-limited voltage follower. With the addition of diodes D1-D2 and D3-D4, it has both a voltage-limited output, and an overvoltage protected input. Operating below the voltage threshold of output series-connected Zener diodes D3-D4, the circuit behaves as a precision voltage follower. Under normal follower operation, that is at input/output voltages $< | V_Z + 0.6 |$ volts (where V_Z is the breakdown voltage of D3 or D4), diodes D1-D2 see only the combined offset and CM voltage errors of U1 as bias voltage. This reduces the D1-D2 leakage to very low levels, consistent with the pA level bias current of a FET input op amp. Note that D1-D2 *must* be prevented from photo-conduction, and one direct means of this is to use opaque package diodes, such as the 2N3906 EB junctions discussed by Pease (see References 3 and 4). If 1N914s are used they must be light shielded. In either case, bootstrapping greatly reduces the effective D1-D2 leakage.

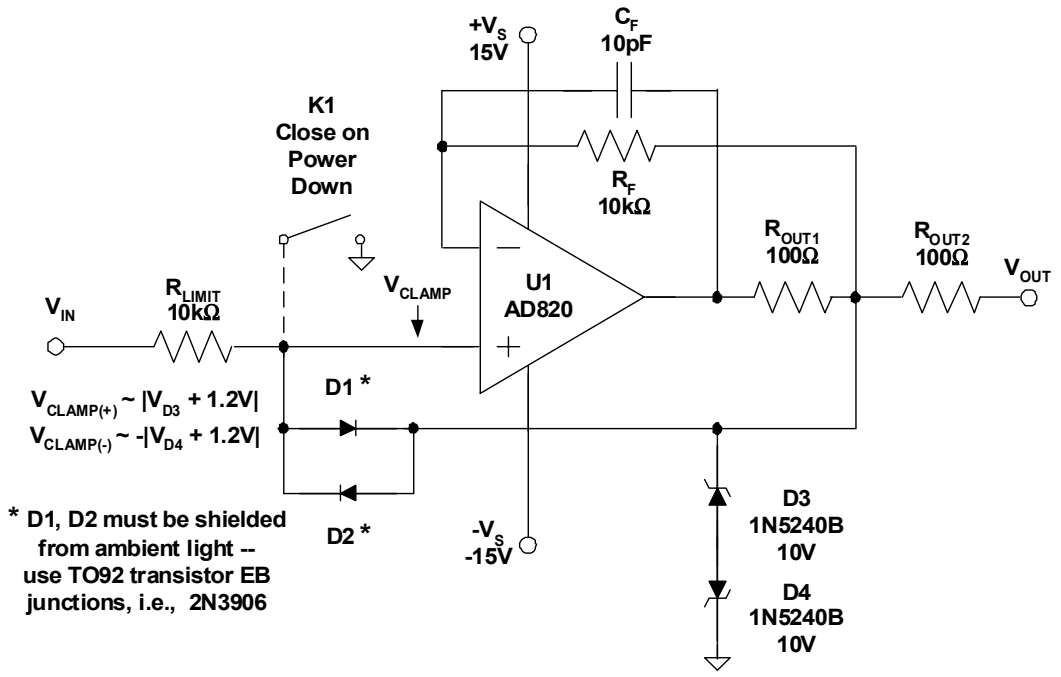


Figure 9.77: *Bootstrapping the D1-D2 Protection Network Reduces Diode Leakage to Negligible Levels, and is Voltage-Programmable for Clamp Level*

For input/output voltage levels greater than V_Z + 0.6 V, Zener diodes D3-D4 breakdown. This action clamps both the V_{OUT} output node and the V_{CLAMP} node via D1-D2. The input of the op amp is clamped to either polarity of the two input levels of V_{CLAMP}, as indicated within the figure. Under clamp conditions, input voltage V_{IN} can rise to levels beyond the supply rails of U1 without harm, with excess current limited by R_{LIMIT}. If sustained high-level (~100 V) inputs will be applied, R_{LIMIT} should be rated as a 1-2 W (or fusible) type.

This circuit has very good dc characteristics, due to the fact that the clamping network is bootstrapped. This produces very low input/output errors below the V_{CLAMP} threshold (consistent with the op amp specifications, of course). Note that this bootstrapping has ac benefits as well, as it reduces the D1-D2 capacitance seen by the source. While the ~100-pF capacitance of D3-D4 might cause a loading problem with some op amps, this is mitigated by the isolating effect of R_{OUT1}, plus the feedback compensation of C_F. Both R_{OUT1} and R_{OUT2} protect the op amp output.

The input voltage clamping level is also programmable, and is set by the choice of Zener voltage V_Z. This voltage plus 1.2 V should be greater than the maximum input, but below the rail voltage, as summarized in the figure. The example uses 10 V ± 5% Zener diodes, so input clamping typically will occur at ±11.2 V, allowing ±10-V swings.

An important caveat to the above is that it applies for *power on* conditions. With *power off*, D1-D4 still clamp to the noted levels, but this now produces a condition whereby the U1 input and output voltage can exceed the rails.

Note that this could be dangerous, for a given U1 device. If so, an optional and simple means towards providing a lower, safe clamping level for power off conditions is to use a

relay at the V_{CLAMP} node. The contacts are open with power applied, and closed with power absent. With attention paid to an overall PCB layout, this can preserve a pA level bias current of FET op amps used for U1.

Common-Mode Overvoltage Protection Using CMOS Channel Protectors

A much simpler alternative for overvoltage protection is the CMOS *channel protector*. A channel protector is a device in series with the signal path, for example preceding an op amp input. It provides overvoltage protection by dynamically altering its resistance under fault conditions. Functionally, it has the distinct advantage of affording protection for sensitive components from voltage transients, whether the power supplies are present or not. Representative devices are the ADG465/ADG466/ADG467, which are channel protectors with single, triple, and octal channel options. Because this form of protection works whether supplies are present or not, the devices are ideal for use in applications where input overvoltages are common, or where correct power sequencing can't always be guaranteed. One such example is within hot-insertion rack systems.

An application of a channel protector for overvoltage protection of a precision buffer circuit is shown in Figure 9.78. A single channel device, the ADG465 at U2, is used here at the input of the U1 precision op amp buffer, an OP777.

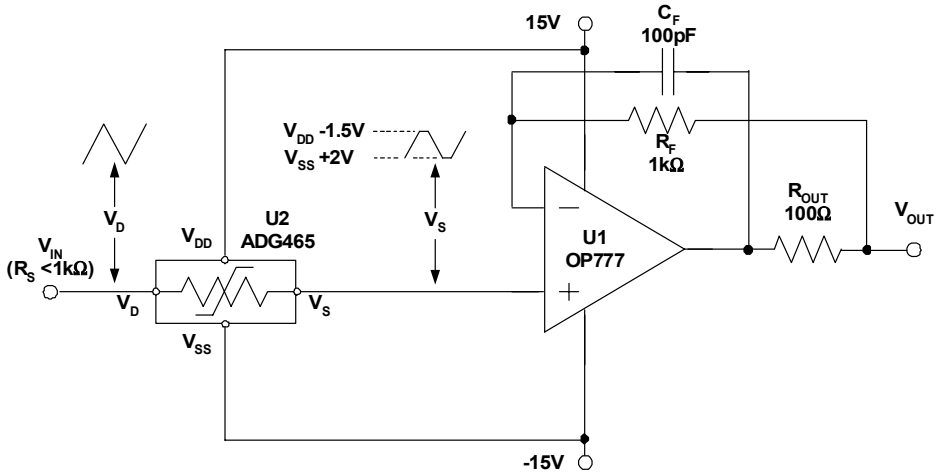


Figure 9.78: *Using an ADG465 Channel Protector IC With a Precision Buffer Offers Great Simplicity of Protection and Fail-Safe Operation During Power Off*

A channel protector behaves just like a series resistor of 60 Ω to 80 Ω in normal operation (i.e., non-fault conditions). Consisting of a series connection of multiple P and N MOSFETs, the protector dynamically adjusts channel resistance according to the voltage seen at the V_D terminal. Normal conduction occurs with V_D more than a threshold level above or below the rails, i.e., $(V_{SS} + 2\ V) < V_D < (V_{DD} - 1.5\ V)$. For fault conditions the analog input voltage exceeds this range, causing one of the series MOSFETs to switch off, thus raising the channel resistance to a high level. This clamps the V_S output at one extreme range, either $V_{SS} + 2$ V or $V_{DD} - 1.5$ V, as shown in Figure 9.78.

A major channel protector advantage is the fact that both circuit and signal source protection are provided, in the event of overvoltage or power loss. Although shown here

operating from op amp ±15-V supplies, these channel protectors can handle total supplies of up to 40 V. They also can withstand overvoltage inputs from V_{SS} – 20 V to V_{DD} + 20 V with power on (or ±35 V in the circuit shown). With power off (V_{DD} = V_{SS} = 0 V), maximum input voltage is ±35 V. Maximum room temperature channel leakage is 1 nA, making them suitable for op amps and in-amps with bias currents of several nA and up.

Related to the ADG46x series of channel protectors are several *fault-protected multiplexers*, for example the ADG508F/509F, and the ADG438F/439F families. Both the channel protectors and the fault-protected multiplexers are low power devices, and even under fault conditions, their supply current is limited to sub microampere levels. A further advantage of the fault-protected multiplexer devices is that they retain proper channel isolation, even for input conditions of one channel seeing an overvoltage, that is the remaining channels still function.

CM Overvoltage Protection Using High CM Voltage In-Amp

The ultimate simplicity for analog channel overvoltage protection is achieved with resistive input attenuation ahead of a precision op amp. This combination equates to a high voltage capable in-amp, such as the AD629, which is able to linearly process differential signals riding upon CM voltages of up to ±270 V. Further, and most important to overvoltage protection considerations, the on-chip resistors afford protection for either common mode or differential voltages of up to ±500 V. All of this is achieved by virtue of a precision laser-trimmed thin-film resistor array and op amp, as shown in Figure 9.79.

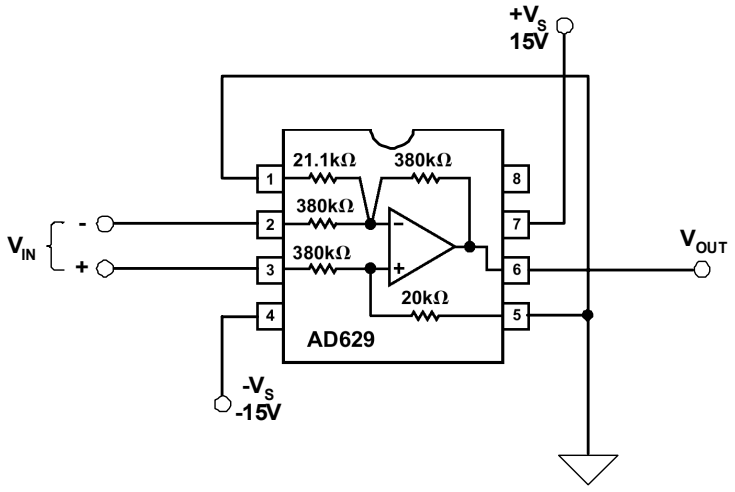


Figure 9.79: *The AD629 High Voltage In-Amp IC Offers ± 500 V Input Overvoltage Protection, One-Component Simplicity, and Fail-Safe Power Off Operation*

Examination of this topology shows that the resistive network around the AD629's precision op amp acts to divide down the applied CM voltage at V_{IN} by a factor of 20/1. The AD629 simultaneously processes the input differential mode signal V_{IN} to a single-ended output referred to a local ground, at a gain factor of unity. Gain errors are no more

than ±0.03 or 0.05%, while offset voltage is no more than 0.5 or 1 mV (grade dependent). The AD629 operates over a supply range of ±2.5 to ±18 V.

These factors combine to make the AD629 a simple, one-component choice for the protection of off-card analog inputs that can potentially see dangerous transient voltages. Due to the relatively high resistor values used, protection of the device is also inherent with no power applied, since the input resistors safely limit fault currents. In addition, it offers those operating advantages inherent to an in-amp: high CMR (86 dB minimum at 500 Hz), excellent overall dc precision, and the flexibility of simple polarity changes.

On the flip side of performance issues, several factors make the AD629's output noise and drift relatively high, if compared to a lower gain in-amp configuration such as the AMP03. These are the Johnson noise of the high value resistors, and the high noise gain of the topology (21×). These factors raise the op amp noise and drift along with the resistor noise by a factor higher than typical. Of course, whether or not this is an issue relevant to an individual application will require evaluation on a case-by-case basis.

Inverting Mode Op Amp Protection Schemes

There are some special cases of overvoltage protection requirements that don't fit into the more general CM protection schemes above. Figure 9.80 is one such example, a low bias current FET input op amp I/V converter.

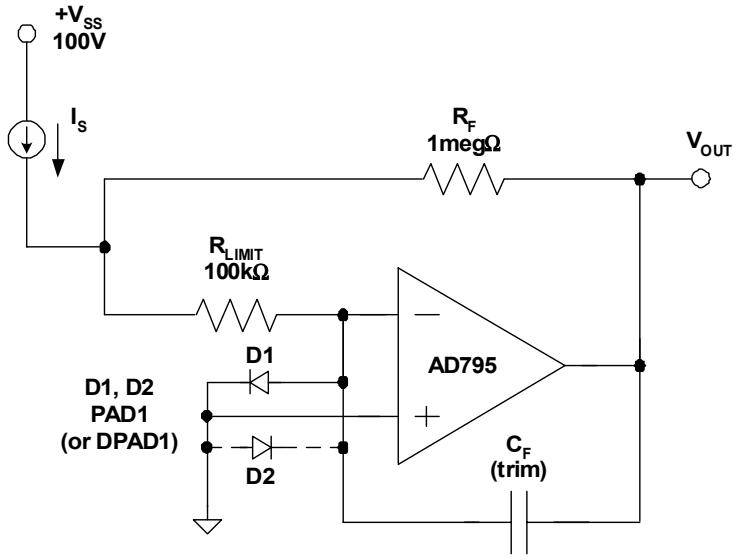


Figure 9.80: *A Low Bias Current FET Input Op Amp I/V Converter With Overvoltage Protection Network R_{LIMIT} and D1*

In this circuit the AD795 1-pA bias current op amp is used as a precision inverter. Some current-source generated signals can originate from a high voltage potential, such as the 100-V V_{SS} level shown. As such, they have the potential of developing fault voltage levels beyond the op amp rails, producing fault current into the op amp well above safe levels. To prevent this, protection resistor R_{LIMIT} is used inside the feedback loop as shown, along with voltage clamp D1 (D2).

For normal signal condition (i.e., $I_S \leq 10\ \mu A$) the op amp's inverting node is very close to ground, with just a tiny voltage drop across R_{LIMIT}. Normal I/V conversion takes place, with gain set by R_F. For protection, D1 is a special low leakage diode, clamping any excess voltage at the (–) node to ~0.6 V, thus protecting the op amp. The value of R_{LIMIT} is chosen to allow a 1-mA max current under fault conditions. Bootstrapping the D1 (and/or D2) clamp diodes as shown minimizes the normal operating voltage across the inverting node, keeping the diode leakage low (see Figure 9.76, again). Note that for a positive source voltage as shown, only positive clamping is needed, so just one diode suffices.

Only the lowest leakage diodes (≤1 pA) such as the PAD1 (or the DPAD1 dual) should be used in this circuit. As noted previously, any clamping diode used here should be shielded from light or use opaque packaging, to minimize photocurrent from ambient light. Even so, the diode(s) will increase the net input current and shunt capacitance, and feedback compensation C_F will likely be necessary to control response peaking. C_F should be a very low leakage type. Also, with the use of very low input bias current devices such as the AD795, it isn't possible to use the same level of internal protection circuitry as with other ADI op amps. This factor makes the AD795 more sensitive to handling, so ESD precautions should be taken.

Amplifier Output Voltage Phase-Reversal

As alluded to above, there are "gray-area" op amp groups that have anomalous CM voltage zones, falling between the supply rails. As such, protection for these devices cannot be guaranteed by simply ensuring that the inputs stay between the rails—they must additionally stay *entirely* within their rated CM range, for consistent behavior.

Peculiar to some op amps, this misbehavior phenomenon is called *output voltage phase-reversal.* It is seen when one or both of the op amp inputs exceeds their allowable input CM voltage range. Note that the inputs may still be well within the extremes of rail voltage, but simply below one specified CM limit. Typically, this is towards the negative range. Phase-reversal is most often associated with JFET and/or BiFET amplifiers, but some bipolar single-supply amplifiers are also susceptible to it.

The Figure 9.81 waveforms illustrates this general phenomenon, with an overdriven voltage follower input on the left, and the resulting output phase-reversal at the right.

While the specific details of the internal mechanism may vary with individual op amps, it suffices to say that the output phase-reversal occurs when a critical section of the amplifier front end saturates, causing the input-output sign relationship to temporarily reverse. Under this condition, when the CM range is exceeded, the negative going input

waveform in Figure 9.81 (left) does not continue going more negative in the output waveform, Figure 9.81 (right). Instead, the input-output relationship *phase-reverses*, with the output suddenly going positive, i.e., the spike. It is important to note that this is *not* a latching form of phase-reversal, as the output will once again continue to properly track the input, when the input returns to the CM range. In Figure 9.81, this can be seen in the continuance of the output sine wave, after the positive-going phase-reversal spike settles.

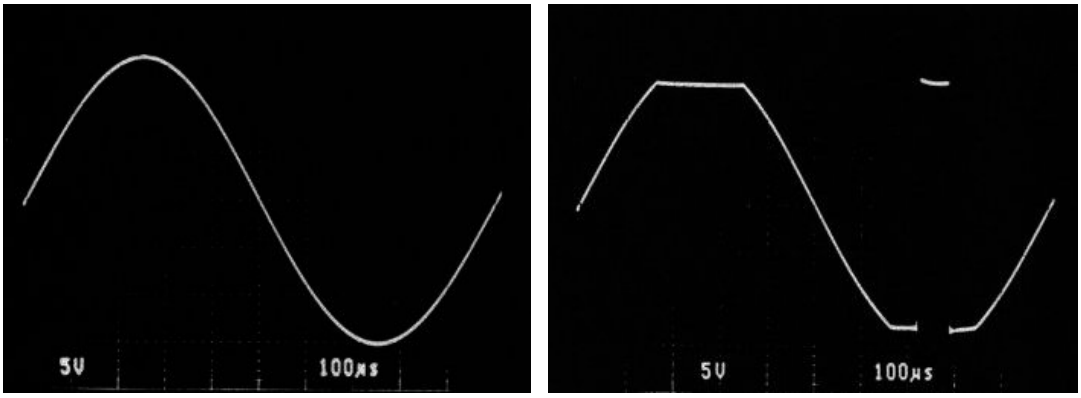


Figure 9.81: *An Illustration of Input Overdriving Waveform (Left) and the Resulting Output Phase-Reversal (Right), Using a JFET Input Op Amp*

In most applications, this output voltage phase-reversal does no harm to the op amp, nor to the circuit where it is used. Indeed, since it is triggered when the CM limit is exceeded, non-inverting stages with appreciable signal gain never see it, since their applied CM voltage is too small.

Note that with inverting applications the output phase-reversal problem is non-existent, as the CM range isn't exercised. So, although a number of (mostly older) op amps suffer from phase-reversal, it still is rarely a serious problem in system design.

Nevertheless, when and if a phase-reversal susceptible amplifier used in a servo loop application sees excess CM voltage, the effect can be disastrous—it goes **Bang!** So, the best advice is to be forewarned.

An Output Phase-Reversal Do-it-Yourself Test

Since output phase-reversal may not always be fully described on a data sheet, it is quite useful to test for it. This is easily done in the lab, by driving a questionable op amp as a unity-gain follower, from a source impedance (R_{LIMIT}) of ~1 kΩ. It is helpful to make this a variable, 1 to 100-kΩ range resistance.

With a low resistance setting (1 kΩ), while bringing the driving signal level slowly up towards the rail limits, observe the amplifier output. If a phase-reversal mechanism is present, when the CM limit of the op amp is exceeded, the output will suddenly reverse (see Figure 9.81, again). If there is no phase-reversal present in an amplifier, the output waveform will simply clip at the limits of its swing. It may prove helpful to have a well-

behaved op amp available for this test, to serve as a performance reference. One such device is the AD8610.

Note that in general, some care should be used with this test. Without a series current-limit resistor, if the generator impedance is too low (or level too high), it could possibly damage an internal junction of the op amp under test. So, obviously, caution is best for such cases.

Once a suitable R_{LIMIT} resistance value is found, well-behaved op amps will simply show a smooth, bipolar range, clipped output waveform when overdriven. This clipping will appear more like the *upper (positive swing)* portion of the waveform within Fig. 9.81, right (again).

Fixes for Output Phase–Reversal

An op amp manufacturer might not always give the R_{LIMIT} resistance value appropriate to prevent output phase-reversal. But, the value can be determined empirically with the driving method mentioned above. Most often, the R_{LIMIT} resistor value providing protection against phase-reversal will also safely limit fault current through any input CM clamping diodes. If in doubt, a nominal value of 1 kΩ is a good starting point for testing.

Typically, FET input op amps will need only the current limiting series resistor for protection, but bipolar input devices are best protected with this same limiting resistor, *along with a Schottky diode* (i.e., R_{LIMIT} and D2, of Figure 9.75, again).

For a more detailed description of the output voltage phase-reversal effect, see References 7 and 8. Figure 9.82 summarizes a number of the key points relating to output voltage phase-reversal.

- ***Non-Latching* Inversion of Transfer Function, Triggered by Exceeding Common Mode Limit**
- **Sometimes Occurs in FET and Bipolar (Single-Supply) Op Amps**
- **Doesn't Harm Amplifier… but *Disastrous* for Servo Systems!**
- **Not Usually Specified on Data Sheet, so Amplifier Must be Checked**
- **Easily Prevented:**
  - **All op amps: Limit applied CM voltage by clamping or other means**
  - **BiFETs: Add series input resistance, R_{LIMIT}**
  - **Bipolars: R_{LIMIT} and Schottky clamp diode to rail**

Figure 9.82: *A Summary of Key Points Regarding Output Phase-Reversal in FET and Bipolar Input Op Amps*

Alternately, any of the several previously mentioned CM clamping schemes can be used to prevent output phase-reversal, by setting the clamp voltage to be less than the amplifier CM range limit where phase-reversal occurs. For example, Figure 9.77 would operate to prevent phase-reversal in FET amplifiers susceptible to it, if the negative clamp limit is set so that $V_{CLAMP(-)}$ never exceeds the typical negative CM range of –11 V on a –15-V rail.

For validation of this or any of the previous overvoltage protection schemes, the circuit should be verified on a number of op amps, over a range of conditions as suitable to the final application environment.

Input Differential Protection

The discussions thus far have been on overvoltage common-mode conditions, which is typically associated with forward biasing of PN junctions inherent in the structure of the input stage. There is another equally important aspect of protection against overvoltage, which is that due to excess *differential* voltages. Excessive differential voltage, when applied to certain op amps, can lead to degradation of their operating characteristics.

This degradation is brought about by *reverse junction breakdown,* a second case of undesirable input stage conduction, occurring under conditions of *differential* overvoltage. However, in the case of reverse breakdown of a PN junction, the problem can be more subtle in nature. It is illustrated by the partial op amp input stage in Figure 9.83

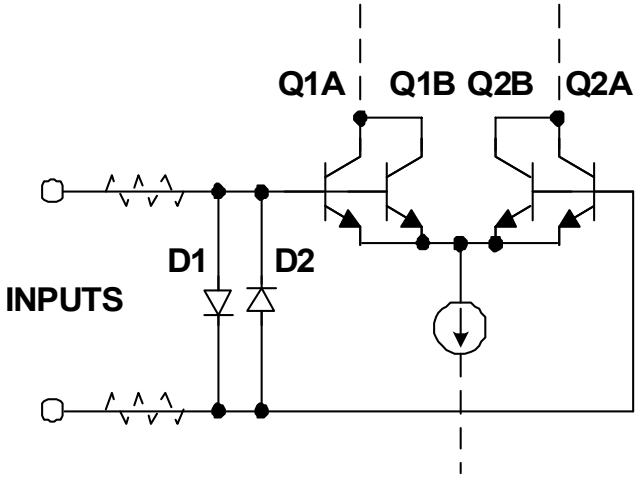


Figure 9.83: *An Op Amp Input Stage With D1-D2 Input Differential Overvoltage Protection Network*

This circuit, applicable to a low noise op amp such as the OP27, is also typical of many others using low noise bipolar transistors for differential pair Q1-Q2. In the absence of any protection, it can be shown that voltages above about 7 V between the two inputs will cause a reverse junction breakdown of either Q2 or Q1 (dependent upon relative polarity). Note that, in cases of emitter-base breakdown, even small reverse currents can cause degradation in both transistor gain and noise (see Reference 6). After emitter-base breakdown occurs, op amp parameters such as the bias currents and noise may well be out of specification. This is usually permanent, and it can occur gradually and quite

subtly, particularly if triggered by transients. For these reasons, virtually all low-noise op amps, whether NPN or PNP based, utilize protection diodes such as D1-D2 across the inputs. These diodes conduct for applied voltages greater than ±0.6 V, protecting the transistors.

The dotted series resistors function as current limiters (protection for the protection diodes) but aren't used in all cases. For example, the AD797 doesn't have the resistors, simply because they would degrade the part's specified noise of 1 nV/√Hz. Note—when the resistors are absent internally, some means of external current limiting must be provided, when and if differential overvoltage conditions do occur. Obviously, this is a tradeoff situation, so the confidence of full protection must be weighed against the noise degradation. Note that an application circuit itself may provide sufficient resistance in the op amp inputs, such that additional resistance isn't needed.

In applying a low noise bipolar input stage op amp, first check the chosen part's data sheet for internal protection. When necessary, protection diodes D1-D2, if not internal to the op amp, should be added to guarantee prevention of Q1-Q2 emitter-base breakdown. If differential transients of more than 5 V can be seen by the op amp in the application, the diodes are in order. Ordinary low capacitance diodes will suffice, such as the 1N4148 family. Add current limiting resistors as necessary, to limit diode current to safe levels.

Other IC device junctions, such as base-collector and JFET gate-source junctions don't exhibit the same degradation in performance upon break down, and for these the input current should be limited to 5 mA, unless the data sheet specifies a different value.

Protecting In-Amps Against Overvoltage

From a protection standpoint, instrumentation amplifiers (in-amps) are similar in many ways to op amps. Like op amps, their absolute maximum ratings must be observed for both common and differential mode input voltages.

A much simplified schematic of the AD620 in-amp is shown in Figure 9.84, showing the input differential transistors and their associated protection parts.

An important point, unique to the AD620 device, is the fact that the 400-Ω internal R_S protection resistors are *thin-film types*. Therefore these resistors don't show symptoms of diode-like conduction to the IC substrate (as would be the case were they diffused resistors). Practically, this means that the input ends of these resistors (pins 3 and 2) can go above or below the supplies. Differential fault currents will be limited by the combination of twice the internal R_S plus the external gain resistance, R_G. Excess applied CM voltages will show current limited by R_S.

In more detail, it can be noted that input transistors Q1 and Q2 have protection diodes D1 and D2 across their base-emitter junctions, to prevent reverse breakdown. For differential voltages, analysis shows that a fault current, I_{IN}, flows through the external R_{LIMIT} resistors (if present), the internal R_S resistors, the gain-setting resistor R_G, and two diode drops (Q2, D1). For the AD620 topology, R_G varies inversely with gain, and a worst case (lowest resistance) occurs with the maximum gain of 1000, when R_G is 49.9 Ω. Therefore the lowest total internal path series resistance is about 850 Ω.

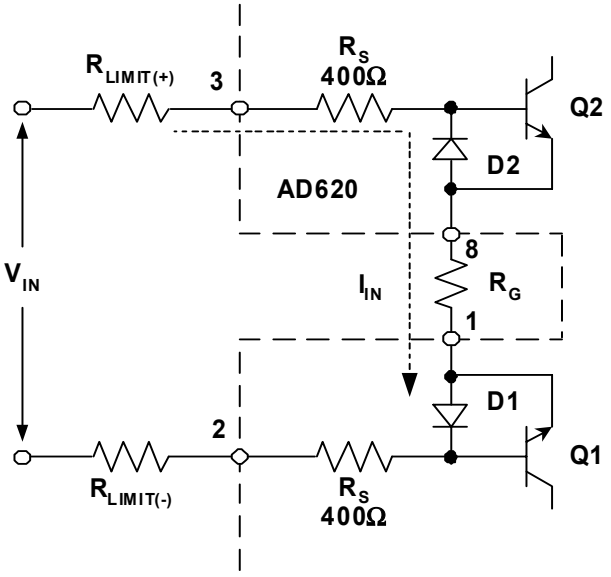


Figure 9.84: *The AD620 In-Amp Input Internally Uses D1-D2 and Series Resistors R_S for Protection (Additional Protection Can Be Added Externally)*

For the AD620, any combination of CM and differential input voltages should be limited to levels that limit the input fault current to 20 mA, maximum. A purely differential voltage of 17 V would result in this current level, for the lowest resistance case. For CM voltages which may go beyond either rail, an internal diode not shown in Fig. 9.84 conducts, effectively clamping the driven input to either $+V_S$ or $-V_S$ at the R_S inner end. For this overvoltage CM condition, the 400-Ω value of R_S and the excess voltage beyond the rail determines the current level. If for example V_{IN} is 23 V with $+V_S$ at 15 V, 8 V appears across R_S, and the 20-mA current rating is reached. Higher fault voltages can be dealt with by adding R_{LIMIT} resistance, to maintain fault current at 20 mA or less.

A more generalized external voltage protection circuit for an in-amp like the AD620 is shown in Figure 9.85.

In this circuit, low-leakage diodes D3-D6 are used as CM clamps. Since the in-amp bias current may be only 1 nA or so (for the AD620), a low-leakage diode type is mandatory. As can be noted from the topology, diode bootstrapping isn't possible with this configuration.

It should be noted that not only must the diodes have basically low leakage, they must also maintain low leakage at the highest expected temperature. This suggests either FET type diodes (see Fig. 9.76, again), or the transistor C-B types shown. The R_{LIMIT} resistors are chosen to limit the maximum diode current under fault conditions. If additional *differential* protection is used, either back-back Zener or Transzorb clamps can be used, shown as D1-D2. If this is done, the leakage and capacitance of these diodes should be carefully considered.

The protection scheme of Figure 9.85, while effective using appropriate parts, has the downside of requiring a number of components. A much more simple in-amp protection using fault protected devices is shown in Figure 9.86. Although shown with an AD620, this circuit is useful with many other dual-supply in-amps with bias currents of 1 nA or more. It uses two-thirds of a triple ADG466 channel-protector for the in-amp differential inputs.

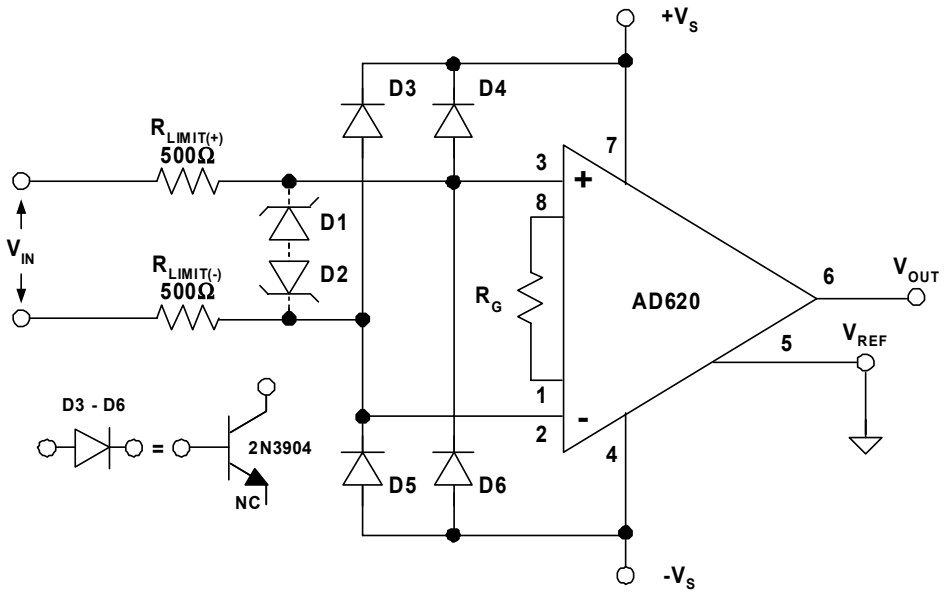


Figure 9.85: *A Generalized Diode Protection Circuit for the AD620 and Other In-Amps Uses D3-D6 for CM Clamping and Series Resistors R_{LIMIT} for Protection*

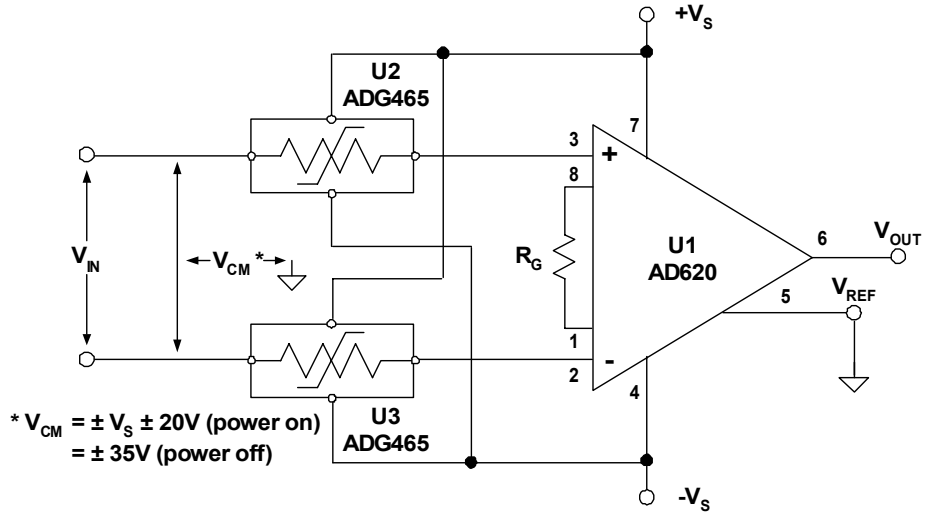


Figure 9.86: *A Channel Protector Device (Or Fault-Protected Multiplexer) Provides Protection for Dual-Supply In-Amps With a Minimum of Extra Parts*

Because the nature of a channel protection device is to turn off as V_{IN} approaches either rail, the scheme of Figure 9.86 doesn't function with rail sensing single-supply in-amps. If near-rail operation and protection is required in an in-amp application, an alternative method is necessary. Many single-supply in-amps are topologically similar to the two-amplifier in-amp circuit which is shown within the dotted box of Figure 9.87.

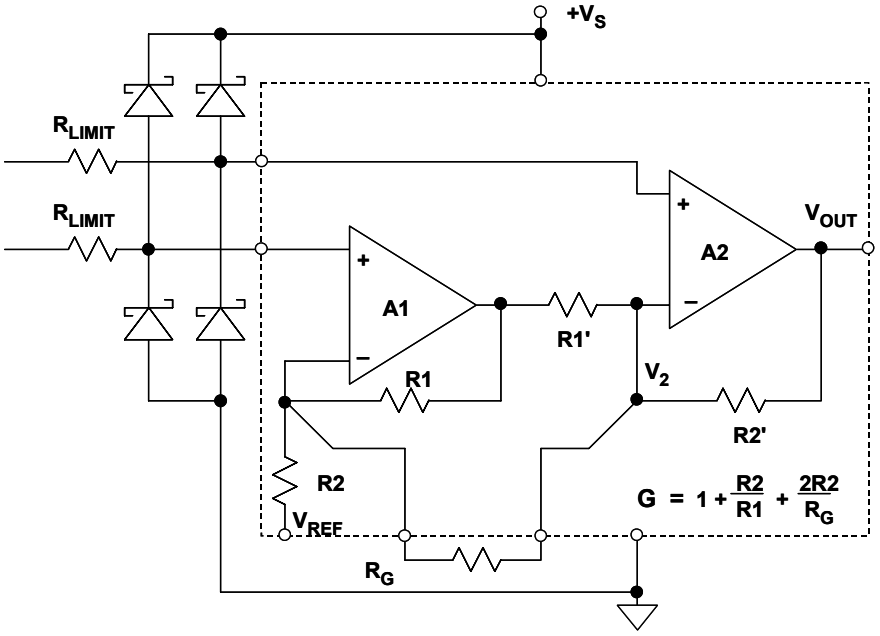


Figure 9.87: *Single-Supply In-Amps May or May Not Require External Protection in the Form of Resistors and Clamp Diodes— If So, They Can Be Added As Shown*

In terms of the necessity for externally added protection components, a given in-amp may or may not require them. Each case needs to be considered individually. For example, some in-amps have clamp diodes as shown, but *internal to the device*. The AD623 is such a part, but it lacks the series resistors, which can be added externally when and if necessary. Note that this approach allows the R_{LIMIT} value to be optimized for protection, with negligible impact on noise for those applications not needing the protection.

Also, some in-amp devices have both internal protection resistors *and* clamping diodes, an example here is the AD627. In this device, the internal protection is adequate for transients up to 40 V beyond the supplies (a 20-mA fault current in the internal resistors). For overvoltage levels higher than this, external R_{LIMIT} resistors can be added.

The use of the Schottky diodes as shown at the two inputs is an option for in-amp protection. If no clamping is specifically provided internally, then they are applicable. Their use is generally similar to the op amp protection case of Figure 9.75, with comparable caveats as far as leakage. Note that in many cases, due to internal protection networks of modern in-amps, these diodes just won't be necessary. But again, there aren't hard rules on this, so always check the data sheet before finalizing an application.

ADCs whose input range falls between the supply rails can generally be protected with external Schottky diodes and a current limit resistor as shown in Figure 9.88. Even if

internal ESD protection diodes are provided, the use of the external ones allows smaller values of R_{LIMIT} and lower noise and offset errors. ADCs with thin-film input attenuators, such as the AD7890-10 (see Figure 9.89), can be protected with Zener diodes or transient voltage suppressors (TVSs) with an R_{LIMIT} resistor to limit the current through them.

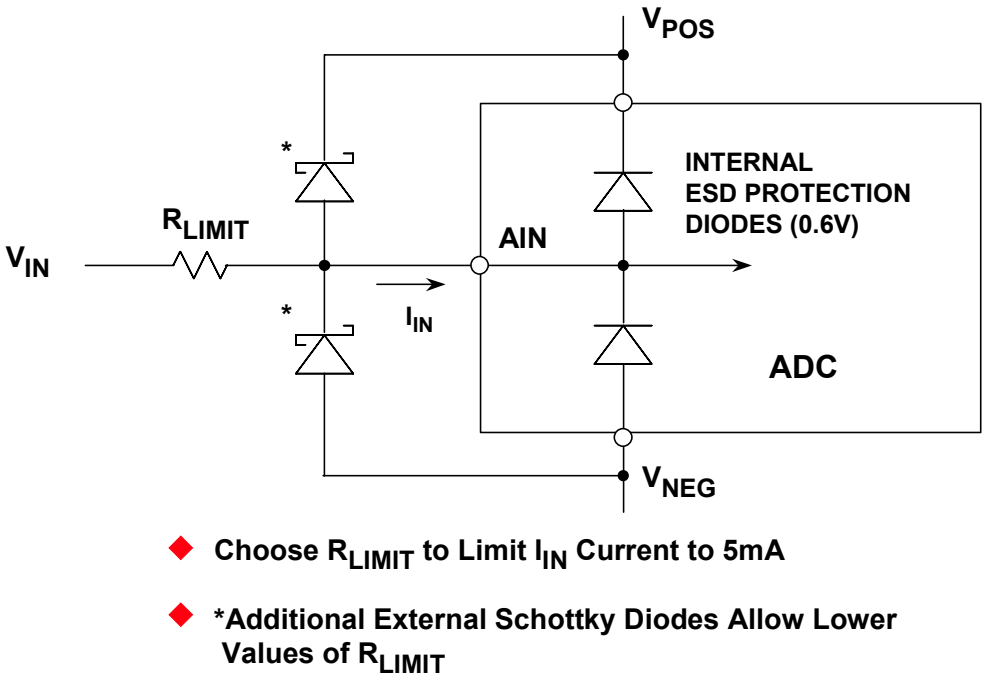


Figure 9.88: *Input Protection for ADCs With Input Ranges Within Supply Voltages*

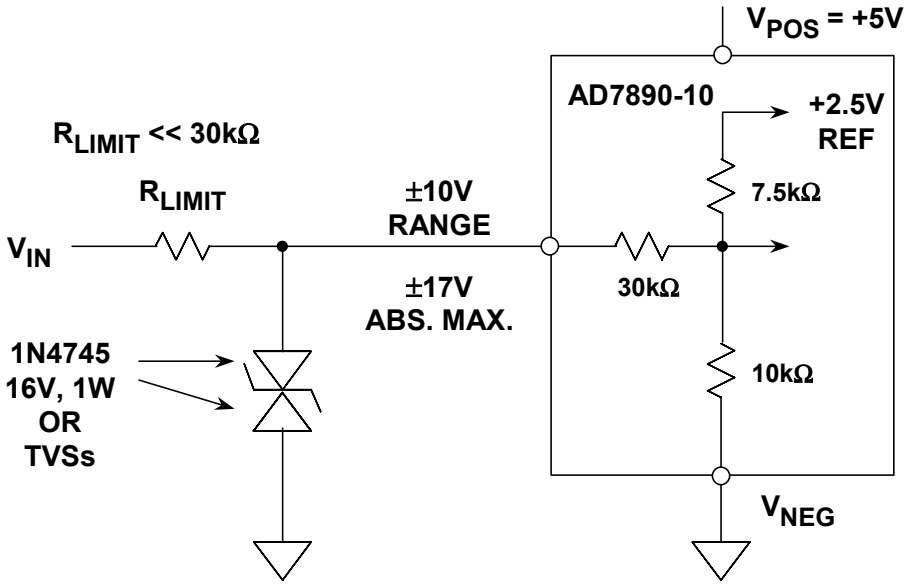


Figure 9.89: *Input Protection for Single-Supply ADCs With Thin Film Resistor Input Attenuators*

Overvoltage Protection Using CMOS Channel Protectors

The ADG465/ADG466/ADG467 are CMOS channel protectors which are placed in series with the signal path. The channel protector will protect sensitive components from voltage transients whether the power supplies are present or not. Because the channel protection works whether the supplies are present or not, the channel protectors are ideal for use in applications where correct power sequencing cannot always be guaranteed (e.g., hot-insertion rack systems) to protect analog inputs.

Each channel protector (see Figure 9.90) has an independent operation and consists of four MOS transistors—two NMOS and two PMOS. One of the PMOS devices does not lie directly in the signal path but is used to connect the source of the second PMOS device to its backgate. This has the effect of lowering the threshold voltage and so increasing the input signal range of the channel for normal operation. The source and backgate of the NMOS devices are connected for the same reason.

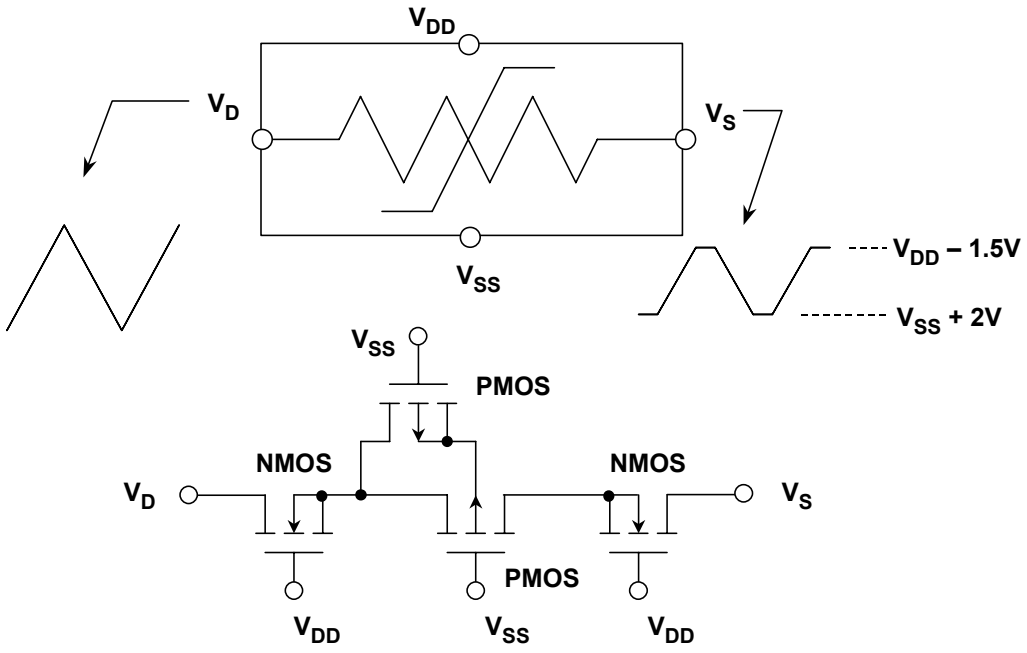


Figure 9.90: *ADG465, ADG466, and ADG467 Single, Triple, and Octal Channel Protectors*

The channel protector behaves just like a series resistor (60 Ω to 80 Ω) during normal operation, i.e., (V_{SS} + 2 V) < V_D < (V_{DD} – 1.5 V). When a channel's analog input voltage exceeds this range, one of the MOSFETs will switch off, clamping the output at either V_{SS} + 2 V or V_{DD} – 1.5 V. Circuitry and signal source protection is provided in the event of an overvoltage or power loss. The channel protectors can withstand overvoltage inputs from V_{SS} – 20 V to V_{DD} + 20 V with power on (V_{DD} – V_{SS} = 44 V maximum). With power off (V_{DD} = V_{SS} = 0 V), maximum input voltage is ±35 V. The channel protectors are very low power devices, and even under fault conditions, the supply current is limited to sub microampere levels. All transistors are dielectrically

isolated from each other using a trench isolation method thereby ensuring that the channel protectors cannot latch up.

Figure 9.91 shows a typical application that requires overvoltage and power supply sequencing protection. The application shows a hot-insertion rack system. This involves plugging a circuit board or module into a live rack via an edge connector. In this type of application it is not possible to guarantee correct power supply sequencing. Correct power supply sequencing means that the power supplies should be connected before any external signals. Incorrect power sequencing can cause a CMOS device to latch up. This is true of most CMOS devices regardless of the functionality. RC networks are used on the supplies of the channel protector to ensure that the rest of the circuit is powered up before the channel protectors. In this way, the outputs of the channel protectors are clamped well below V_{DD} and V_{SS} until the capacitors are charged. The diodes ensure that the supplies on the channel protector never exceed the supply rails when it is being disconnected. Again this ensures that signals on the inputs of the CMOS devices never exceed the supplies.

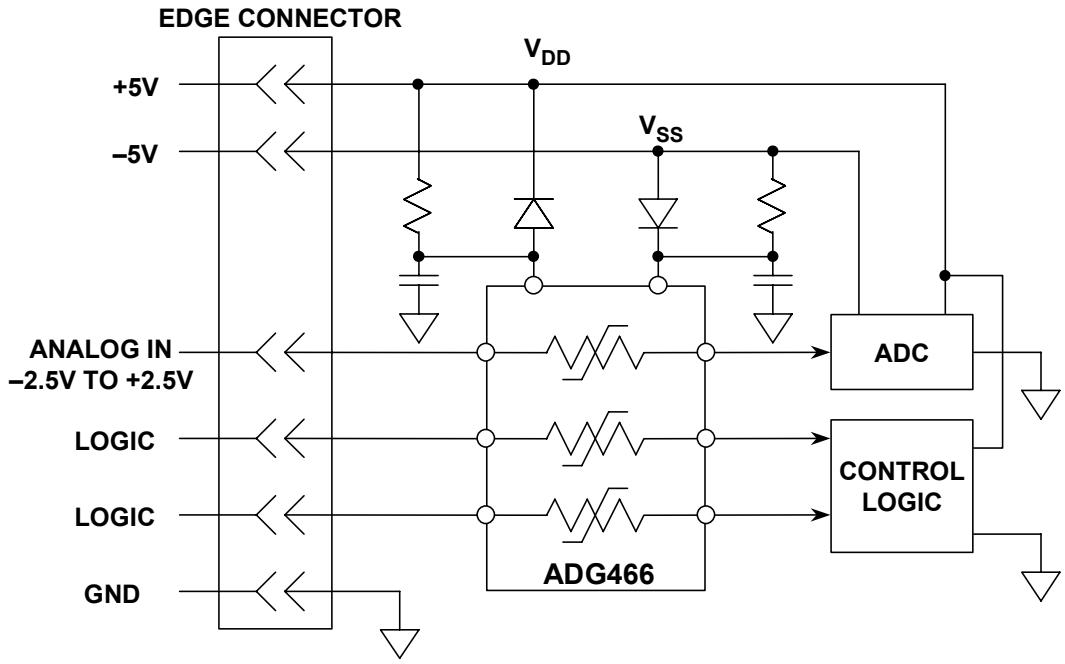
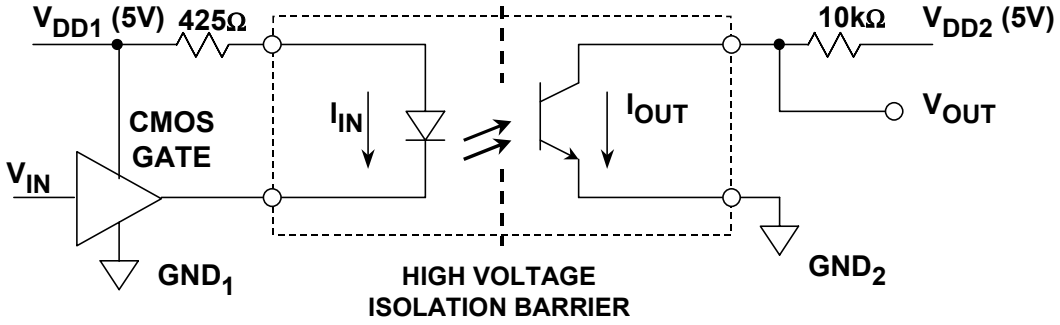


Figure 9.91: *Overvoltage and Power Supply Sequencing Protection Using the ADG466*

Digital Isolators

One way to break ground loops is to use digital isolation techniques. Analog isolation amplifiers find many applications where a high degree of isolation is required, such as in medical instrumentation. Digital isolation techniques offer a reliable method of transmitting digital signals over interfaces with high common-mode voltages without introducing ground noise.

Optocouplers (also called optoisolators) are useful and available in a wide variety of styles and packages. A typical optocoupler based on an LED and a phototransitor is shown in Figure 9.92. A current of approximately 10 mA is applied to an LED transmitter, and the light output is received by a phototransistor. The light produced by the LED is sufficient to saturate the phototransistor. Isolation of 5000 V rms to 7000 V rms is common. Although excellent for digital signals, optocouplers are too nonlinear for most analog applications. One should also realize that since the phototransistor is operated in a saturated mode, rise and fall-times can range from 10 µs to 20 µs in slower devices, thereby limiting applications at high speeds.



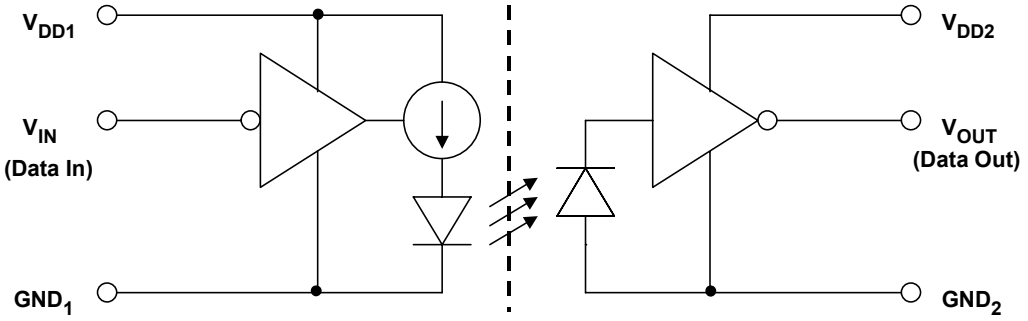
- **Uses Light for Transmission Over a High Voltage Barrier**
- **The LED is the Transmitter, and the Phototransistor is the Receiver**
- **High Voltage Isolation: 5000V to 7000V RMS**
- **Non-Linear -- Best for Digital or Frequency Information**
- **Rise and Fall-times can be 10 to 20µs in Slower Devices**
- **Example: Siemens ILQ-1 Quad (http://www.siemens.com)**

Figure 9.92: *Digital Isolation Using LED / Phototransistor Optocouplers*

A faster optocoupler architecture is shown in Figure 9.93 and is based on an LED and a photodiode. The LED is again driven with a current of approximately 10 mA. This produces a light output sufficient to generate enough current in the receiving photodiode to develop a valid high logic level at the output of the transimpedance amplifier. Speed can vary widely between optocouplers, and the fastest ones have propagation delays of 20 ns typical, and 40 ns maximum, and can handle data rates up to 25 Mbps for NRZ data. This corresponds to a maximum square wave operating frequency of 12.5 MHz, and a minimum allowable passable pulse width of 40 ns.

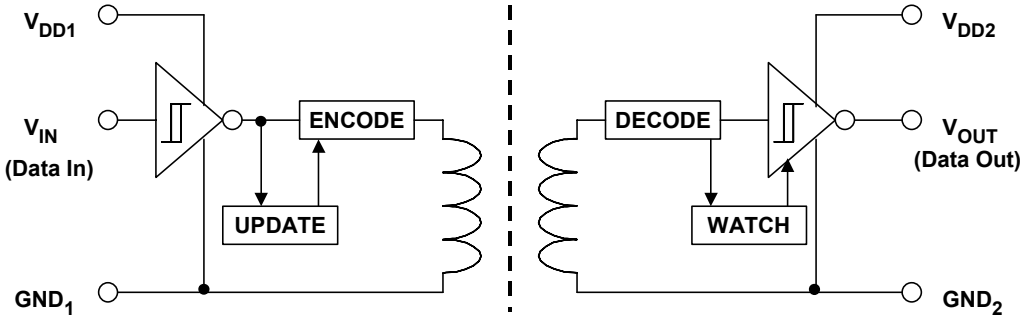
The ADuM1100A and ADuM1100B are digital isolators based on Analog Devices' *i*Coupler® technology. Combining high speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics superior to the traditional optocouplers previously described.

Configured as pin-compatible replacements for existing high speed optocouplers, the ADuM1100A and ADuM1100B support data rates as high as 25 Mbps and 100 Mbps, respectively. A functional diagram of the devices is shown in Figure 9.94.



- +5V Supply Voltage
- 2500V RMS I/O Withstand Voltage
- Logic Signal Frequency: 12.5MHz Maximum
- 25Mbps Maximum Data Rate
- 40ns Maximum Propagation Delay
- 9ns Typical Rise/Fall Time
- Example: Agilent HCPL-7720
  (http://www.semiconductor.agilent.com)

Figure 9.93: *Digital Isolation Using LED / Photodiode Optocouplers*



ADuM1100

- +5V/+3.3V Supply Voltage
- 2500V RMS I/O Withstand Voltage
- 100 Mbps Maximum Data Rate (ADuM1100B)
- 18ns Maximum Propagation Delay
- 3ns Typical Rise/Fall Time
- Pin Compatible with Popular Optocouplers

ADuM1300/ADuM1400

- 3 Channel: ADuM1300, 4 Channel: ADuM1400
- +2.7V to +5.5V Supply Voltage
- Logic Level Translation Capability
- 2500V RMS I/O Withstand Voltage
- 100 Mbps Maximum Data Rate (ADuM1300C, ADuM1400C)
- 32ns Maximum Propagation Delay (ADuM1300C, ADuM1400C)
- 3ns Typical Rise/Fall Time

Figure 9.94: *ADuM1100A/ADuM1100B Digital Isolators*

Both the ADuM1100A and ADuM1100B operate at either 3.3-V or 5-V supply voltages, have propagation delays < 18 ns, edge asymmetry of <2 ns, and rise and fall-times <3 ns. They operate at very low power, less than 900 μA of quiescent current (sum of both sides) and a dynamic current of less than 160 μA per Mbps of data rate. Unlike common transformer implementations, the parts provide dc correctness with a patented refresh feature which continuously updates the output signal.

The ADuM1300/ADuM1301 digital isolators offer 3 channels of isolation, and the ADuM1400/ADuM1401 isolators offer 4 channels of isolation. These devices operate from +2.7 V to + 5.5 V and have independent input and output power inputs allowing them to operate not only as isolators but also as logic level translators.

The AD260/AD261 family of digital isolators isolates five digital control signals to/from high speed DSPs, microcontrollers, or microprocessors. The AD260 also has a 1.5-W transformer for a 3.5-kV rms isolated external dc/dc power supply circuit.

Each line of the AD260 can handle digital signals up to 20 MHz (40 Mbps) with a propagation delay of only 14 ns which allows for extremely fast data transmission. Output waveform symmetry is maintained to within ±1 ns of the input so the AD260 can be used to accurately isolate time-based pulse width modulator (PWM) signals.

A simplified schematic of one channel of the AD260/AD261 is shown in Figure 9.95. The data input is passed through a schmitt trigger circuit, through a latch, and a special transmitter circuit which differentiates the edges of the digital input signal and drives the primary winding of a proprietary transformer with a "set-high/set-low" signal. The secondary of the isolation transformer drives a receiver with the same "set-hi/set-low" data which regenerates the original logic waveform. An internal circuit operates in the background which interrogates all inputs about every 5 μs and in the absence of logic transitions, sends appropriate "set-hi/set-low" data across the interface. Recovery time from a fault condition or at power-up is thus between 5 μs and 10 μs.

The power transformer (available on the AD260) is designed to operate between 150 kHz and 250 kHz and will easily deliver more than 1 W of isolated power when driven push-pull (5 V) on the transmitter side. Different transformer taps, rectifier and regulator schemes will provide combinations of ±5 V, 15 V, 24 V, or even 30 V or higher. The output voltage when driven with a low voltage-drop drive will be 37 V p-p across the entire secondary with a 5-V push-pull drive. Key specifications for the parts are given in Figure 9.96.

To summarize, Figure 9.97 reviews the major points of the in-circuit overvoltage issues discussed in this section.

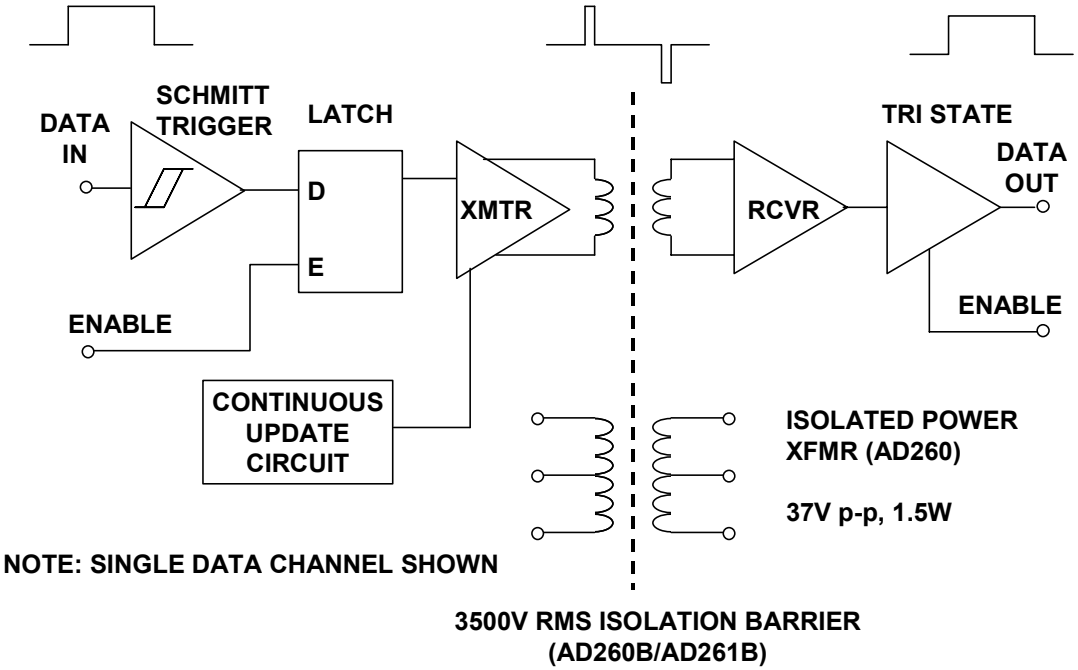


Figure 9.95: *AD260/AD261 Digital Isolators*

- **Isolation Test Voltage to 3500V RMS (AD260B/AD261B)**
- **Five Isolated Digital Lines Available in 6 Input/Output Configurations**
- **Logic Signal Frequency: 20MHz Max.**
- **Data Rate: 40Mbps Max.**
- **Isolated Power Transformer: 37V p-p, 1.5W (AD260)**
- **Waveform Edge Transmission Symmetry: ±1ns**
- **Propagation Delay: 14ns**
- **Rise and Fall-Times < 5ns**

Figure 9.96: *AD260/AD261 Digital Isolator Key Specifications*

- **INPUT VOLTAGES MUST NOT EXCEED ABSOLUTE MAXIMUM RATINGS (Usually Specified With Respect to Supply Voltages)**
- **Requires $V_{IN(CM)}$ Stay Within a Range Extending to ≤0.3V Beyond Rails ($-V_S-0.3V \geq V_{IN} \leq +V_S+0.3V$)**
- **IC Input Stage Fault Currents *Must* Be Limited (≤ 5mA Unless Otherwise Specified)**
- **Avoid Reverse-Bias Breakdown in Input Stage Junctions!**
- **Differential and Common Mode Ratings Often Differ**
- **No Two Amplifiers are Exactly the Same**
- **Watch Out for Output Phase-Reversal in JFET and SS Bipolar Op Amps!**
- **Some ICs Contain *Internal* Input Protection**
  - **Diode Voltage Clamps, Current Limiting Resistors (or both)**
  - **Absolute Maximum Ratings Must Still Be Observed**

Figure 9.97: *A summary of In-Circuit Overvoltage Points*

If these varied overvoltage precautions for op amps and in-amps seem complex, yes indeed, they are! Whenever op amp (or in-amp or data converter) inputs (and outputs) go outside equipment boundaries, dangerous or destructive things can happen to them. Obviously, these potentially hazardous situations should be anticipated, for highest reliability.

Fortunately, most applications are contained entirely within the equipment, and usually see inputs and outputs to/from other ICs on the same power system. Therefore clamping and protection schemes typically aren't necessary for these cases.

Out-of-Circuit Overvoltage Protection

Linear ICs such as op amps, in-amps, and data converters must also be protected prior to the time that they are mounted to a printed circuit board. That is an *out-of-circuit* state. In such a condition, ICs are completely at the mercy of their environment as to what stressful voltage surges they may see. Most often the harmful voltage surges come from *electrostatic discharge,* or, as more commonly referenced, ESD. This is a single, fast, high current transfer of electrostatic charge resulting from one of two conditions. These conditions are:

1) Direct contact transfer between two objects at different potentials (sometimes called contact discharge)

2) A high electrostatic field between two objects when they are in close proximity (sometimes called air discharge)

The prime sources of static electricity are mostly insulators and are typically synthetic materials, e.g., vinyl or plastic work surfaces, insulated shoes, finished wood chairs, Scotch tape, bubble pack, soldering irons with ungrounded tips, etc. Voltage levels generated by these sources can be extremely high since their charge is not readily

distributed over their surfaces or conducted to other objects. The generation of static electricity caused by rubbing two substances together is called the *triboelectric* effect. Some common examples of ordinary acts producing significant ESD voltages are shown in Figure 9.98.

- **Walking Across a Carpet**
  1000V - 1500V
- **Walking Across a Vinyl Floor**
  150V - 250V
- **Handling Material Protected by Clear Plastic Covers**
  400V - 600V
- **Handling Polyethylene Bags**
  1000V - 2000V
- **Pouring Polyurethane Foam Into a Box**
  1200V - 1500V
- **Note: Above Assumes 60% RH. For Low RH (30%), Voltages Can Be > 10 Times**

Figure 9.98: *ESD Voltages Generated By Various Ordinary Circumstances*

ICs can be damaged by the high voltages and high peak currents generated by ESD. Precision analog circuits, often featuring very low bias currents, are more susceptible to damage than common digital circuits, because traditional input-protection structures which protect against ESD damage increase input leakage—and thus can't be used.

For the design engineer or technician, the most common manifestation of ESD damage is a catastrophic failure of the IC. However, exposure to ESD can also cause increased leakage or degrade other parameters. If a device appears to not meet a data sheet specification during evaluation, the possibility of ESD damage should be considered. Figure 9.99 outlines some relevant points on ESD induced failures.

All ESD-sensitive devices are shipped in protective packaging. ICs are usually contained in either conductive foam or antistatic shipping tubes, and the container is then sealed in a static-dissipative plastic bag. The sealed bag is marked with a distinctive sticker, such as in Figure 9.100, which outlines the appropriate handling procedures.

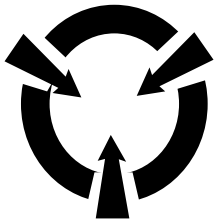
The presence of outside package notices such as those shown in Figure 9.100 is notice to the user that device handling procedures appropriate for ESD protection are necessary.

In addition, data sheets for ESD-sensitive ICs generally have a bold statement to that effect, as shown in Figure 9.101.

- **ESD Failure Mechanisms:**
  - **Dielectric or junction damage**
  - **Surface charge accumulation**
  - **Conductor fusing**
- **ESD Damage Can Cause:**
  - **Increased leakage**
  - **Degradation in performance**
  - **Functional failures of ICs**
- **ESD Damage is often Cumulative:**
  - **For example, each ESD "zap" may increase junction damage until, finally, the device fails.**

Figure 9.99: *Understanding ESD damage*

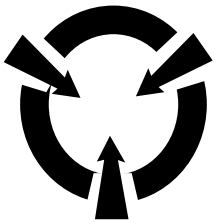
All static sensitive devices are sealed in protective packaging and marked with special handling instructions



CAUTION

SENSITIVE ELECTRONIC DEVICES

DO NOT SHIP OR STORE NEAR STRONG ELECTROSTATIC, ELECTROMAGNETIC, MAGNETIC, OR RADIOACTIVE FIELDS

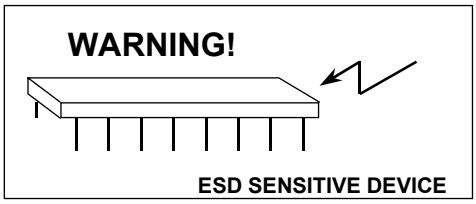


CAUTION

SENSITIVE ELECTRONIC DEVICES

DO NOT OPEN EXCEPT AT APPROVED FIELD FORCE PROTECTIVE WORK STATION

Figure 9.100: *Recognizing ESD-Sensitive Devices by Package and Labeling*



CAUTION

ESD (Electrostatic Discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADXXX features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Figure 9.101: *ESD Data Sheet Statement for Linear ICs*

Once ESD-sensitive devices are identified, protection is relatively easy. Obviously, keeping ICs in their original protective packages as long as possible is a first step. A second step is discharging potentially damaging ESD sources before IC damage occurs. Discharging such voltages can be done quickly and safely, through a high impedance.

A key component required for ESD-safe IC handling is a workbench with a static-dissipative surface, shown in the workstation of Figure 9.102. The surface is connected to ground through a 1-MΩ resistor, which dissipates any static charge, while protecting the user from electrical ground fault shock hazards. If existing bench tops are nonconductive, a static-dissipative mat should be added, along with the discharge resistor.

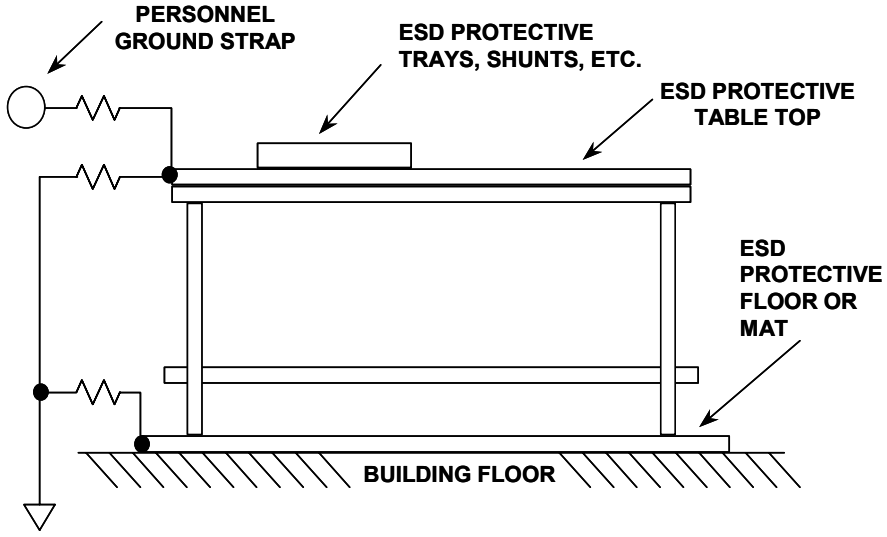


Figure 9.102: *A Workstation Environment Suitable for Handling ESD-Sensitive ICs*

Note that the surface of the workbench has a moderately high sheet resistance. It is neither necessary nor desirable to use a low-resistance surface (such as a sheet of copper-clad PC board) for the work surface. Remember, a high peak current may flow if a charged IC is discharged through a low impedance. This is precisely what happens when a charged IC contacts a grounded copper clad board. When the same charged IC is placed on the high impedance surface of Figure 9.102 however, the peak current isn't high enough to damage the device.

Several personnel handling techniques are keys to minimizing ESD-related damage. At the workstation, a conductive wrist strap is recommended while handling ESD-sensitive devices. The wrist strap ensures that normal tasks, such as peeling tape from packages, won't cause IC damage. Again, a 1-MΩ resistor, from the wrist strap to ground, is required for safety. When building prototype breadboards or assembling PC boards which contain ESD-sensitive ICs, all passive components should be inserted and soldered before the ICs. This minimizes the ESD exposure of the sensitive devices. The soldering iron must, of course, have a grounded tip.

Protecting ICs from ESD requires the participation of both the IC manufacturer and the customer. IC manufacturers have a vested interest in providing the highest possible level of ESD protection for their products. IC circuit designers, process engineers, packaging specialists and others are constantly looking for new and improved circuit designs, processes, and packaging methods to withstand or shunt ESD energy.

A complete ESD protection plan, however, requires more than building ESD protection into ICs. The users of ICs must also provide their employees with the necessary knowledge of and training in ESD handling procedures, so that protection can be built in at all key points along the way, as outlined in Figure 9.103.

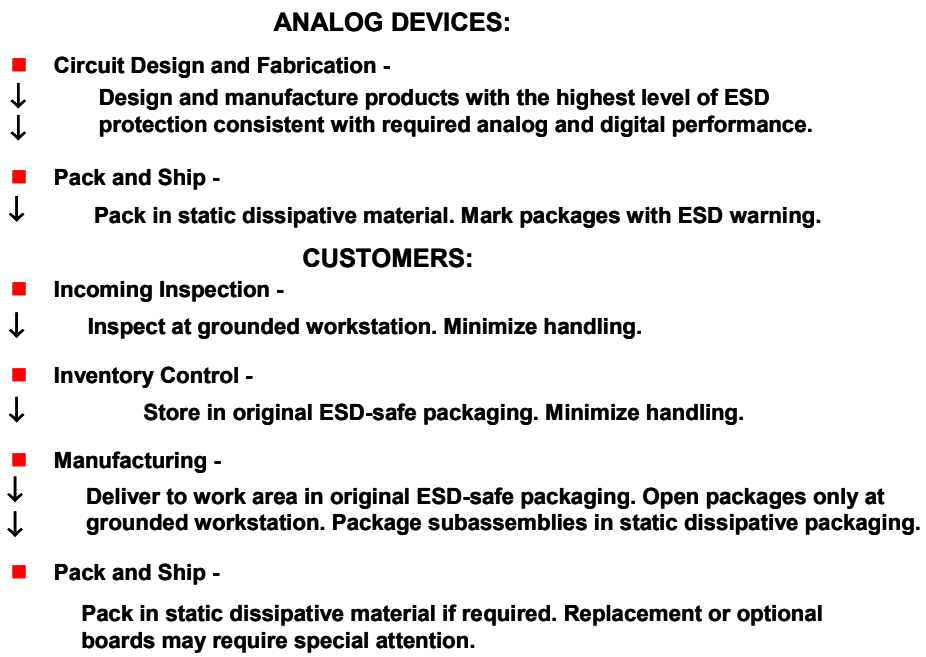


Figure 9.103: *ESD Protection Requires a Partner Relationship Between ADI and the End Customer With Control at Key Points*

Special care should be taken when breadboarding and evaluating ICs. The effects of ESD damage can be cumulative, so repeated mishandling of a device can eventually cause a failure. Inserting and removing ICs from a test socket, storing devices during evaluation, and adding or removing external components on the breadboard should all be done while observing proper ESD precautions. Again, if a device fails during a prototype system development, repeated ESD stress may be the cause.

The key word to remember with respect to ESD is *prevention*. There is no way to undo ESD damage, or to compensate for its effects.

ESD Models and Testing

Some applications have higher sensitivity to ESD than others. ICs which are located on a PC board surrounded by other circuits are generally much less susceptible to ESD damage than circuits which must interface with other PC boards or the outside world. These ICs are generally not specified or guaranteed to meet any particular ESD specification (with the exception of MIL-STD-883 Method 3015 classified devices). A good example of an ESD-sensitive interface is the RS-232 interface port ICs on a computer, which can easily be exposed to excess voltages. In order to guarantee ESD performance for such devices, the test methods and limits must be specified.

A host of test waveforms and specifications have been developed to evaluate the susceptibility of devices to ESD. The three most prominent of these waveforms currently in use for semiconductor or discrete devices are: The Human Body Model (HBM), the Machine Model (MM), and the Charged Device Model (CDM). Each of these models represents a fundamentally different ESD event, consequently, correlation between the test results for these models is minimal.

Since 1996, all electronic equipment sold to or within the European Community must meet Electromechanical Compatibility (EMC) levels as defined in specification IEC1000-4-x. Note that this does not apply to individual ICs, *but to the end equipment.* These standards are defined along with test methods in the various IEC1000 specifications, and are listed in Figure 9.104.

IEC1000-4-2 specifies compliance testing using two coupling methods, *contact discharge* and *air-gap discharge*. Contact discharge calls for a direct connection to the unit being tested. Air-gap discharge uses a higher test voltage, but does not make direct contact with the unit under test. With air discharge, the discharge gun is moved toward the unit under test, developing an arc across the air gap, hence the term air discharge. This method is influenced by humidity, temperature, barometric pressure, distance and rate of closure of the discharge gun. The contact-discharge method, while less realistic, is more repeatable and is gaining acceptance in preference to the air-gap method.

- **IEC1000-4 Electromagnetic Compatibility EMC**
- **IEC1000-4-1 Overview of Immunity Tests**
- **IEC1000-4-2 Electrostatic Discharge Immunity (ESD)**
- **IEC1000-4-3 Radiated Radio-Frequency Electromagnetic Field Immunity**
- **IEC1000-4-4 Electrical Fast Transients (EFT)**
- **IEC1000-4-5 Lightening Surges**
- **IEC1000-4-6 Conducted Radio Frequency Disturbances above 9kHz**
- **Compliance Marking:** CE

Figure 9.104: *A Listing of the IEC Standards Applicable to ESD Specifications and Testing Procedures*

Although very little energy is contained within an ESD pulse, the extremely fast risetime coupled with high voltages can cause failures in unprotected ICs. Catastrophic destruction can occur immediately as a result of arcing or heating. Even if catastrophic failure does not occur immediately, the device may suffer from parametric degradation, which may result in degraded performance. The cumulative effects of continuous exposure can eventually lead to complete failure.

I-O lines are particularly vulnerable to ESD damage. Simply touching or plugging in an I-O cable can result in a static discharge that can damage or completely destroy the interface product connected to the I-O port (such as RS-232 line drivers and receivers).

Traditional ESD test methods such as MIL-STD-883B Method 3015.7 do not fully test a product's susceptibility to this type of discharge. This test was intended to test a product's susceptibility to ESD damage during handling. Each pin is tested with respect to all other pins. There are some important differences between the MIL-STD-883B Method 3015.7 test and the IEC test, noted as follows:

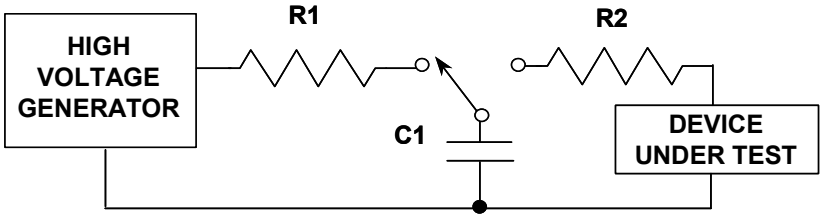
1) The IEC test is much more stringent in terms of discharge energy. The peak current injected is over four times greater.

2) The current risetime is significantly faster in the IEC test.

3) The IEC test is carried out while power is applied to the device.

It is possible that ESD discharge could induce latch-up in the device under test. This test is therefore more representative of a real-world I-O discharge where the equipment is operating normally with power applied. For maximum confidence, however, both tests should be performed on interface devices, thus ensuring maximum protection both during handling, and later, during field service.

A comparison of the test circuit values for the IEC1000-4-2 model versus the MIL-STD-883B Method 3015.7 Human Body Model is shown in Figure 9.105.

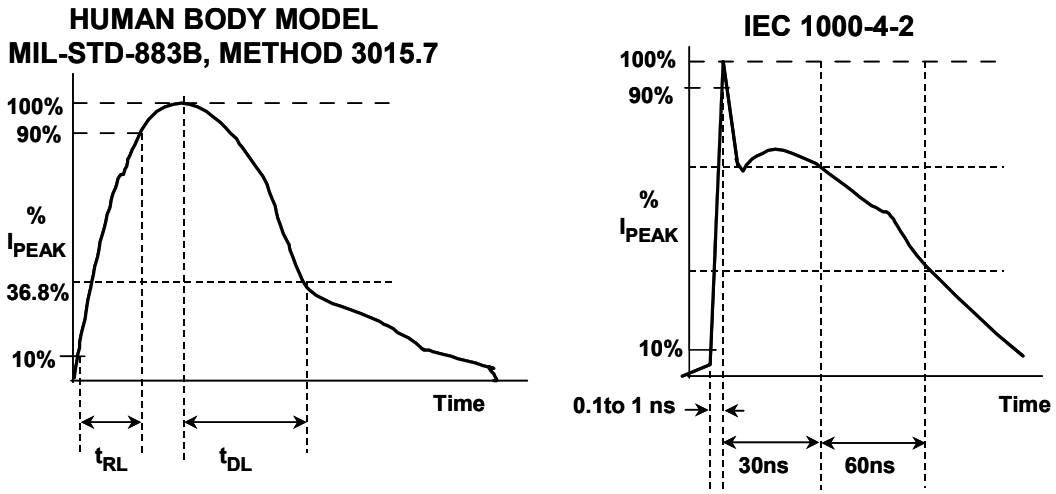


ESD TEST METHOD	R2	C1
Human Body Model MIL STD 883B Method 3015.7	1.5kΩ	100pF
IEC 1000-4-2	330Ω	150pF

NOTE: CONTACT DISCHARGE VOLTAGE SPEC FOR IEC 1000-4-2 IS ±8kV

Figure 9.105: *ESD Test Circuits and Values*

The ESD waveforms for the MIL-STD-883B, METHOD 3015.7 and IEC 1000-4-2 tests are compared in Figure 9.106, left and right, respectively.



- **Voltage : 8 kV**
- **Peak Current :**
  - **MIL-883B, Method 3015.7 HBM : 5 A**
  - **IEC 1000-4-2 : 25 A**

Figure 9.106: *ESD Test Waveforms*

Suitable ESD-protection design measures are relatively easy to incorporate, and most of the overvoltage protection methods already discussed in this section will help. Additional protection can also be obtained. For RS-232 and RS-485 drivers and receivers, the ADMXXX-E series is supplied with guaranteed 15-kV (HBM) ESD specifications. For more general uses, the addition of TransZorbs at appropriate places in a system can provide protection against ESD (see References).

Figure 9.107 summarizes the major points about ESD prevention, from both an out-of-circuit as well as an in-circuit perspective.

- **Observe all Absolute Maximum Ratings on Data Sheet!**
- **Read ADI AN-397 (See Reference 16)**
- **Purchase ESD-Specified Digital Interface Devices**
  - **ADMXXX-E Series of RS-232 / RS-485 Drivers / Receivers (See Reference 18)**
- **Follow General Over-voltage Protection Recommendations**
  - **Add Series Resistance to Limit Currents**
  - **Add Zeners or Transient Voltage Suppressors (TVS) for Extra Protection (See Reference 19)**

Figure 9.107: *A Summary of ESD Points*

REFERENCES:
9.4 OVERVOLTAGE PROTECTION

1. Walt Kester, Wes Freeman, Joe Buxton, "Overvoltage Protection," portion of Section 10 within Walt Kester, Editor, **Practical Design Techniques for Sensor Signal Conditioning**, Analog Devices, Inc., 1999, ISBN 0-916550-20-6.

2. Siliconix PAD/JPAD/SSTPAD series Low leakage Pico-Amp Diodes, Vishay/Siliconix, http://www.vishay.com/brands/siliconix/SSFsglld.html

3. Bob Pease, "Bounding, Clamping Techniques Improve Circuit Performance," **EDN**, November 10, 1983, p. 277.

4. Bob Pease, "Understanding Diodes and Their Problems," Chapter 6 within **Troubleshooting Analog Circuits**, Butterworth-Heinemann, 1991, ISBN 0-7506-9184-0.

5. Dov Kurz, Avner Cohen, "Bootstrapping Reduces Amplifier Input Capacitance," **EDN**, March 20, 1978.

6. C.D. Motchenbacher, J.A. Connelly, Chapter 5, within **Low Noise Electronic System Design**, John Wiley, 1993.

7. Adolfo Garcia**, "**Operational Amplifier Output Voltage Phase Reversal**,"** Section 11, pp. 1-10 within Walt Kester, Editor, **1992 Amplifier Applications Guide**, Analog Devices, Inc., Norwood, MA, 1992, ISBN 0-916550-10-9.

8. Adolfo Garcia**,** Wes Freeman*,* "Overvoltage Effects On Analog Integrated Circuits**,"** Section 7 within Walt Kester, Editor, **Practical Analog Design Techniques**, Analog Devices, Inc., Norwood, MA, 1995, ISBN 0-916550-16-8.

9. Charles Kitchen, Lew Counts, **A Designer's Guide to Instrumentation Amplifiers**, Analog Devices, Inc., 2000.

10. Walt Kester, Wes Freeman, James Bryant, "Electrostatic Discharge," portion of Section 10 within Walt Kester, Editor, **Practical Design Techniques for Sensor Signal Conditioning**, Analog Devices, Inc., 1999, ISBN 0-916550-20-6.

11. MIL-STD-883 Method 3015, "Electrostatic Discharge Sensitivity Classification." Available from Standardization Document Order Desk, 700 Robbins Ave., Building #4, Section D, Philadelphia, PA, 19111-5094.

12. EIAJ ED-4701 Test Method C-111, "Electrostatic Discharges." Available from the Japan Electronics Bureau, 250 W 34th St., New York NY 10119, Attn.: Tomoko.

13. ESD Association Standard S5.2 for "Electrostatic Discharge (ESD) Sensitivity Testing -Machine Model (MM)- Component Level." Available from the ESD Association, Inc., 200 Liberty Plaza, Rome, NY 13440.

14. ESD Association Draft Standard DS5.3 for "Electrostatic Discharge (ESD) Sensitivity Testing - Charged Device Model (CDM) Component Testing." Available from the ESD Association, Inc., 200 Liberty Plaza, Rome, NY 13440.

15. **ESD Prevention Manual**, Analog Devices, Inc.

16. Niall Lyne, "Electrically Induced Damage to Standard Linear Integrated Circuits: The Most Common Causes and the Associated Fixes to Prevent Reoccurrence," **Analog Devices AN397**.

17. Mike Bryne, "How to Reliably Protect CMOS Circuits Against Power Supply Overvoltaging," **Analog Devices AN311**.

18. Data sheet for **ADM3311E RS-232 Port Transceiver**, Analog Devices, Inc., http://www.analog.com

19. TransZorbs are available from General Semiconductor, Inc., 10 Melville Park Road, Melville, NY, 11747-3113, (631) 847-3000, http://www.gensemi.com/product/categories/tvs/tvs.htm

SECTION 9.5: THERMAL MANAGEMENT

Walt Jung

For reliability reasons, data converter systems handling appreciable power are increasingly called upon to observe *thermal management*. All semiconductors have some specified safe upper limit for junction temperature (T_J), usually on the order of 150°C (sometimes 175°C). Like maximum power supply voltages, maximum junction temperature is a worst case limitation which must not be exceeded. In conservative designs, it won't be approached by less than an ample safety margin. Note that this is critical, since semiconductor lifetime is inversely related to operating junction temperature. Simply put, the cooler ICs are, the more they can approach their maximum life.

This limitation of power and temperature is basic, and is illustrated by a typical data sheet statement as in Figure 9.108. In this case it is for the AD8017AR, an 8-pin SOIC device.

> ***The maximum power that can be safely dissipated by the AD8017 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated device is determined by the glass transition temperature of the plastic, approximately +150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of +175°C for an extended period can result in device failure.***

Figure 9.108: *Maximum Power Dissipation Data Sheet Statement for the AD8017AR, an ADI Thermally Enhanced SOIC Packaged Device*

Tied to these statements are certain conditions of operation, such as the power dissipated by the device, and the package mounting specifics to the printed circuit board (PCB). In the case of the AD8017AR, the part is rated for 1.3 W of power at an ambient of 25°C. This assumes operation of the 8-lead SOIC package on a two-layer PCB with about 4 in^2 (~2500 mm^2) of 2 oz. copper for heat sinking purposes. Predicting safe operation for the device under other conditions is covered below.

Thermal Basics

The symbol θ is generally used to denote *thermal resistance*. Thermal resistance is in units of °C/watt (°C/W). Unless otherwise specified, it defines the resistance heat encounters transferring from a hot IC junction to the ambient air. It might also be expressed more specifically as θ_{JA}, for *thermal resistance, junction-to-ambient*. θ_{JC} and θ_{CA} are two additional θ forms used, and are further explained below.

In general, a device with a thermal resistance θ equal to 100°C/W will exhibit a temperature differential of 100°C for a power dissipation of 1 W, as measured between two reference points. Note that this is a linear relationship, so 1 W of dissipation in this part will produce a 100°C differential (and so on, for other powers). For the AD8017AR example, θ is about 95°C/W, so 1.3 W of dissipation produces about a 124°C junction-to-

ambient temperature differential. It is of course this rise in temperature that is used to predict the internal temperature, in order to judge the thermal reliability of a design. With the ambient at 25°C, this allows an internal junction temperature of about 150°C. In practice most ambient temperatures are above 25°C, so less power can then be handled.

For any power dissipation P (in watts), one can calculate the effective temperature differential (ΔT) in °C as:

$$\Delta T = P \times \theta \qquad \text{Eq. 9.10}$$

where θ is the total applicable thermal resistance.

Figure 9.109 summarizes a number of basic thermal relationships.

- **θ = Thermal Resistance (°C/W)**
- **P = Total Device Power Dissipation (W)**
- **T = Temperature (°C)**
- **ΔT = Temperature Differential = P × θ**
- **θ_{JA} = Junction-Ambient Thermal Resistance**
- **θ_{JC} = Junction-Case Thermal Resistance**
- **θ_{CA} = Case-Ambient Thermal Resistance**
- **$\theta_{JA} = \theta_{JC} + \theta_{CA}$**
- **$T_J = T_A + (P \times \theta_{JA})$**
- ***Note: $T_{J(Max)}$ = 150°C (Sometimes 175°C)***

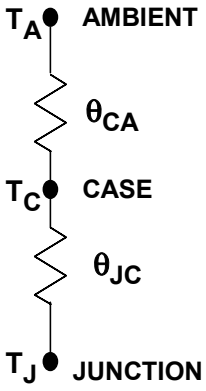


Figure 9.109: *Basic Thermal Relationships*

Note that series thermal resistances, such as the two shown at the right, model the total thermal resistance path a device may see. Therefore the total θ for calculation purposes is the sum, i.e., $\theta_{JA} = \theta_{JC}$ and θ_{CA}. Given the ambient temperature T_A, P, and θ, then T_J can be calculated. As the relationships signify, to maintain a low T_J, either θ or the power being dissipated (or both) must be kept low. A low ΔT is the key to extending semiconductor lifetimes, as it leads to lower maximum junction temperatures.

In ICs, one temperature reference point is always the device junction, taken to mean the hottest spot inside the chip operating within a given package. The other relevant reference point will be either T_C, the case of the device, or T_A, that of the surrounding air. This then leads in turn to the above mentioned individual thermal resistances, θ_{JC} and θ_{JA}.

Taking the most simple case first, θ_{JA} is the thermal resistance of a given device measured between its *junction* and the *ambient* air. This thermal resistance is most often used with small, relatively low power ICs such as op amps, which often dissipate 1 W or less. Generally, θ_{JA} figures typical of op amps and other small devices are on the order of 90-100°C/W for a plastic 8 pin DIP package, as well as the better SOIC packages.

It should be clearly understood that these thermal resistances are *highly* package dependent, as different materials have different degrees of thermal conductivity. As a general guideline, thermal resistance of conductors is analogous to electrical resistances, that is copper is the best, followed by aluminum, steel, and so on. Thus copper lead frame packages offer the highest performance, i.e., the lowest θ.

Heat Sinking

By definition, a *heat sink* is an added low thermal resistance device attached to an IC to aid heat removal. A heat sink has additional thermal resistance of its own, θ_{CA}, rated in °C/W. However, most current op amp packages don't easily lend themselves to heat sink attachment (exceptions are older TO-99 metal can types). Devices meant for heat sink attachment will often be noted by a θ_{JC} dramatically lower than the θ_{JA}. In this case θ will be composed of more than one component. Thermal impedances add, making a net calculation relatively simple. For example, to compute a net θ_{JA} given a relevant θ_{JC}, the thermal resistance of the heat sink, θ_{CA}, or *case* to *ambient* is added to the θ_{JC} as:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \qquad \text{Eq. 9.11}$$

and the result is the θ_{JA} for that specific circumstance.

More generally however, modern ICs *don't* use commercially available heat sinks. Instead, when significant power needs to be dissipated, such as ≥1 W, low thermal resistance copper PCB traces are used as the heat sink. In such cases, the most useful form of manufacturer data for this heat sinking are the boundary conditions of a sample PCB layout, and the resulting θ_{JA} for those conditions. This is in fact the type of specific information supplied for the AD8017AR, as mentioned earlier. Applying this approach, example data illustrating thermal relationships for such conditions is shown by Figure 9.110. These data apply for an AD8017AR mounted to a heat sink with an area of about 4 square inches on a 2 layer, 2 ounce copper PCB.

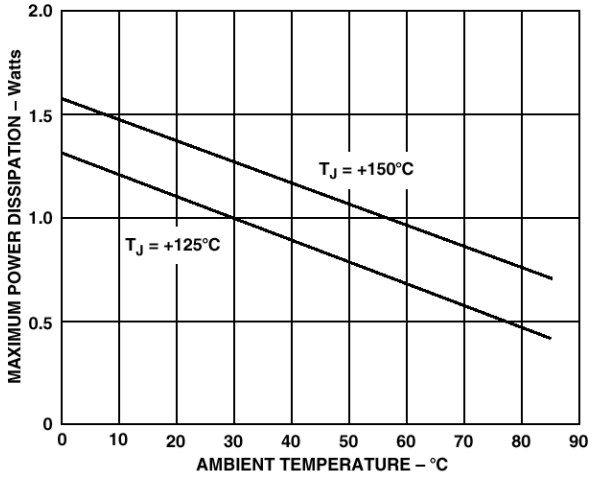


Figure 9.110: *Thermal Rating Curves for AD8017AR Op Amp*

These curves indicate the maximum power dissipation vs. temperature characteristic for the AD8017, for maximum junction temperatures of both 150°C and 125°C. Such curves are often referred to as *derating* curves, since allowable power decreases with ambient temperature.

With the AD8017AR, the proprietary ADI *Thermal Coastline* IC package is used, which allows additional power to be dissipated with no increase in the SO-8 package size. For a $T_{J(max)}$ of 150°C, the upper curve shows the allowable power in this package, which is 1.3 W at an ambient of 25°C. If a more conservative $T_{J(max)}$ of 125°C is used, the lower of the two curves applies.

A performance comparison for an 8-pin standard SOIC and the ADI Thermal Coastline version is shown in Figure 9.111. Note that the Thermal Coastline provides an allowable dissipation at 25°C of 1.3 W, whereas a standard package allows only 0.8 W. In the Thermal Coastline heat transferal is increased, accounting for the package's lower θ_{JA}.

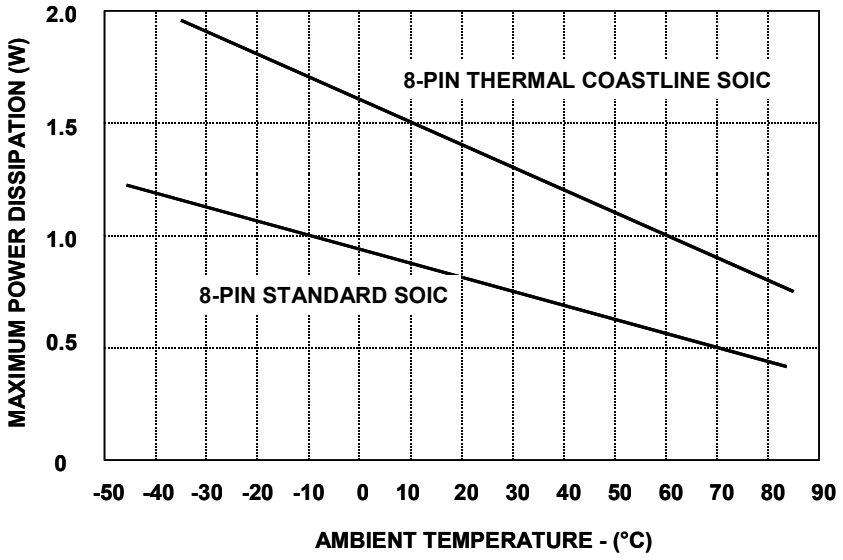


Figure 9.111: *Thermal Rating Curves for Standard (Lower) and ADI Thermal Coastline (Upper) 8-Pin SOIC Packages*

Even higher power dissipation is possible, with the use of IC packages better able to transfer heat from chip to PCB. An example is the AD8016 device, available with two package options rated for 5.5 and 3.5 W at 25°C, respectively, as shown in Figure 9.112.

Taking the higher rated power option, the AD8016ARP PSOP3 package, when used with a 10 inch^2 1 oz. heat sink plane, the combination is able to handle up to 3 W of power at an ambient of 70°C, as noted by the upper curve. This corresponds to a θ_{JA} of 18°C/W, which in this case applies for a maximum junction temperature of 125°C.

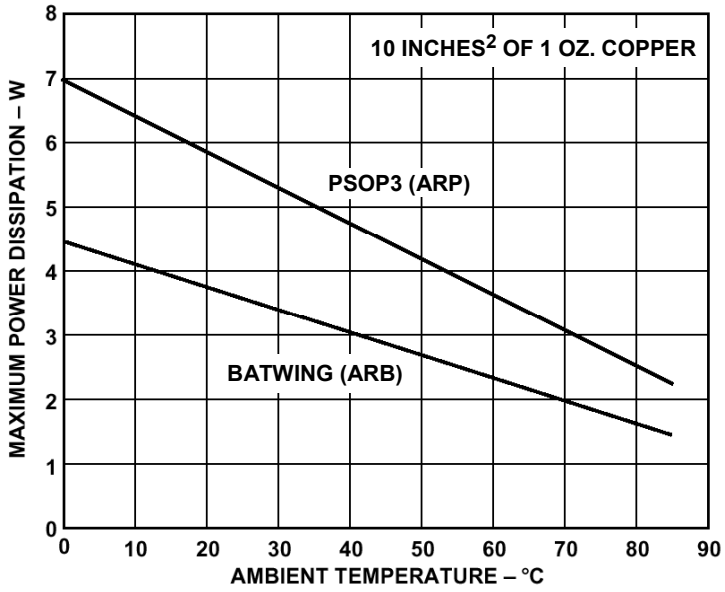


Figure 9.112: *Thermal Characteristic Curves for the AD8016 BATWING (Lower) and PSOP3 (Upper) Packages, for $T_{J(Max)}$ Equal to 125°C*

The reason the PSOP3 version of the AD8016 is so better able to handle power lies with the use of a large area copper slug. Internally, the IC die rest directly on this slug, with the bottom surface exposed as shown in Figure 9.113. The intent is that this surface be soldered directly to a copper plane of the PCB, thereby extending the heat sinking.

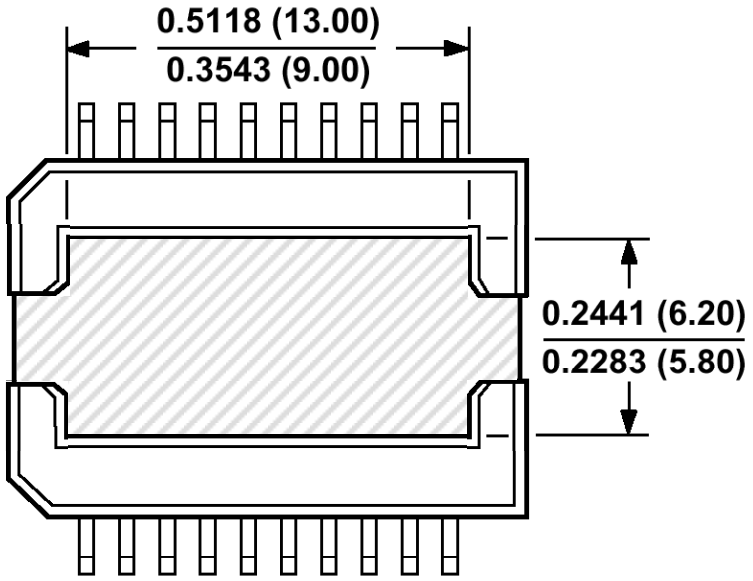


Figure 9.113: *Bottom View of AD8016 20-Lead PSOP3 Package Showing Copper Slug for Aid in Heat Transfer (Central Grayed Area)*

Both of the AD8016 package options are characterized for both still and moving air, but the thermal information given above applies *without* the use of directed airflow. Therefore, adding additional airflow lowers thermal resistance further (see Reference 2).

For reliable, low thermal resistance designs with op amps, several design *Do's and Don'ts* are listed below. Consider all of these points, as may be practical.

1) *Do use as large an area of copper as possible for a PCB heat sink, up to the point of diminishing returns.*

2) *In conjunction with 1), do use multiple (outside) PCB layers, connected together with multiple vias.*

3) *Do use as heavy copper as is practical (2 oz. or more preferred).*

4) *Do provide sufficient natural ventilation inlets and outlets within the system, to allow heat to freely move away from hot PCB surfaces.*

5) *Do orient power-dissipating PCB planes vertically, for convection-aided airflow across heat sink areas.*

6) *Do consider the use of external* power buffer *stages, for precision op amp applications.*

7) *Do consider the use of* forced air, *for situations where several watts must be dissipated in a confined space.*

8) *Don't use solder mask planes over heat dissipating traces.*

9) *Don't use excessive supply voltages on ICs delivering power.*

For the most part, these points are obvious. However, one that could use some elaboration is number 9. Whenever an application requires only modest *voltage* swings (such as for example standard video, 2 V p-p) a wide supply voltage range can often be used. But, as the data of Figure 9.114 indicates, operation of an op amp driver on higher supply voltages produces a large IC dissipation, even though the load power is constant.

In such cases, as long as the distortion performance of the application doesn’t suffer, it can be advantageous to operate the IC on lower supplies, say ±5 V, as opposed to ±15 V. The above example data was calculated on a dc basis, which will generally tax the driver more in terms of power than a sine wave or a noise-like waveform, such as a DMT signal (see Reference 2). The general principles still hold for these ac waveforms, i.e., the op amp power dissipation is high when load current is high and the voltage low.

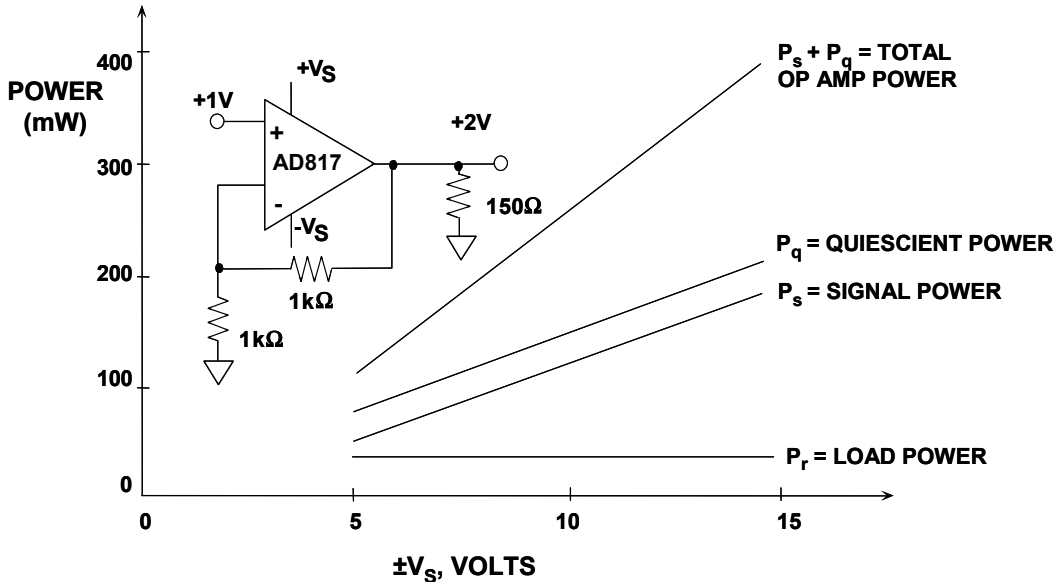


Figure 9.114: *Power Dissipated in Video Op Amp Driver for Various Supply Voltages With Low Voltage Output Swing*

While there is ample opportunity for high power handling with the thermally enhanced packages described above for the AD8016 and AD8017, the increasingly popular smaller IC packages actually move in an opposite direction. Without question, it is true that today's smaller packages do noticeably sacrifice thermal performance. But, it must be understood that this is done in the interest of realizing a smaller size for the packaged op amp, and, ultimately, a much greater final PCB density for the overall system.

These points are illustrated by the thermal ratings for the AD8057 and AD8058 family of single and dual op amp devices, as is shown in Figure 9.115. The AD8057 and AD8058 op amps are available in three different packages. These are the SOT-23-5, and the 8-pin µSOIC, along with standard SOIC.

As the data shows, as the package size becomes smaller and smaller, much less power is capable of being removed. Since the lead frame is the only heatsinking possible with such tiny packages, their thermal performance is thus reduced. The θ_{JA} for the packages mentioned is 240, 200, and 160°C/W, respectively. Note this is more of a *package* than *device* limitation. Other ICs with the same packages have similar characteristics.

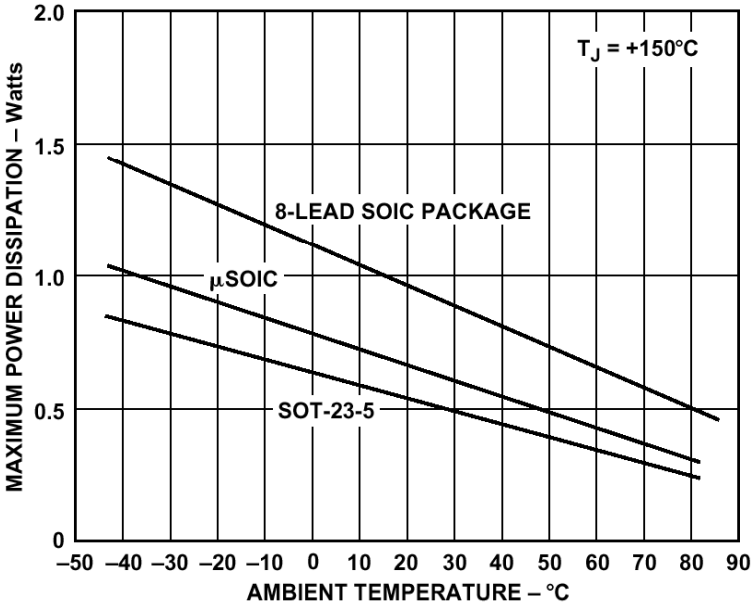


Figure 9.115: *Comparative Thermal Performance for Several AD8057/58 Op Amp Package Options*

Data Converter Thermal Considerations

At first glance, one might assume that the power dissipation of an ADC or a DAC will remain constant for a given power supply voltage. However, many data converters, especially CMOS ones, have power dissipations that are highly dependent upon not only output data loading but also the sampling clock frequency. Since many of the newer high-speed converters can dissipate between 1.5 and 2 W maximum power under the worst case operating conditions, this point must be well understood in order to ensure that the package is mounted in such a way as to maintain the junction temperature within acceptable limits at the highest expected operating temperature.

The previous discussion in this chapter on grounding emphasized that the digital outputs of high performance ADCs, especially those with parallel outputs, should be lightly loaded (5-10 pF) in order to prevent digital transient currents from corrupting the SNR and SFDR. Even under light output loading, however, most CMOS and BiCMOS ADCs have power dissipations which are a function of sampling clock frequency and in some cases, the analog input frequency and amplitude.

For example, Figure 9.116 shows the AD9245 14-bit, 80-MSPS, 3-V CMOS ADC power dissipation versus frequency for a 2.5-MHz analog input and 5-pF output loading of the data lines. The graphs show the digital and analog power supply currents separately as well as the total power dissipation. Note that total power dissipation can vary between approximately 310 mW and 380 mW as the sampling frequency is varied between 10 and 80 MSPS.

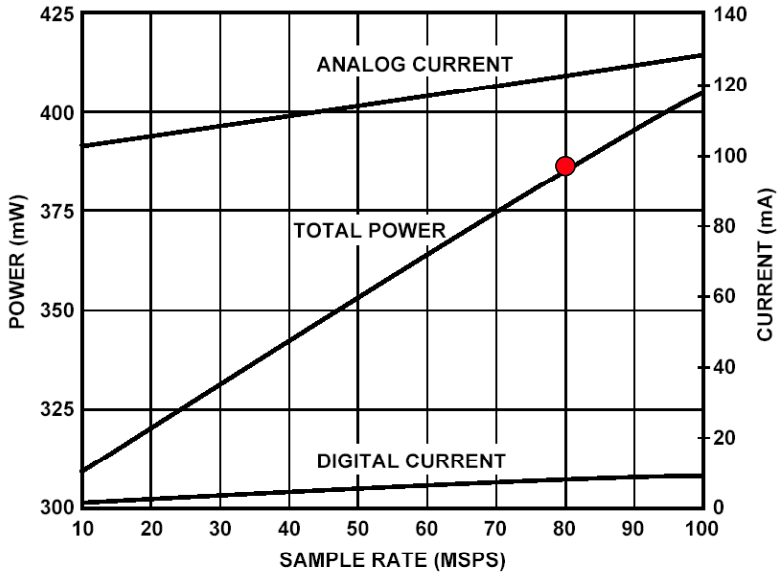


Figure 9.116: *AD9245 14-Bit, 80-MSPS, 3-V CMOS ADC Power Dissipation vs. Sample Rate for 2.5-MHz Input, 5-pF Output Loads*

The AD9245 is packaged in a 32-pin leadless chip scale package as shown in Figure 9.117. The bottom view of the package shows the exposed paddle which should be soldered to the PC board ground plane for best thermal transfer. The worst-case package junction-to-ambient resistance, θ_{JA}, is specified as 32.5°C/W, which places the junction 32.5°C × 0.38 = 12.3°C above the ambient for a power dissipation of 380 mW. For a maximum operating temperature of +85°C, this places the junction at a modest 85°C + 12.3°C = 97.3°C.

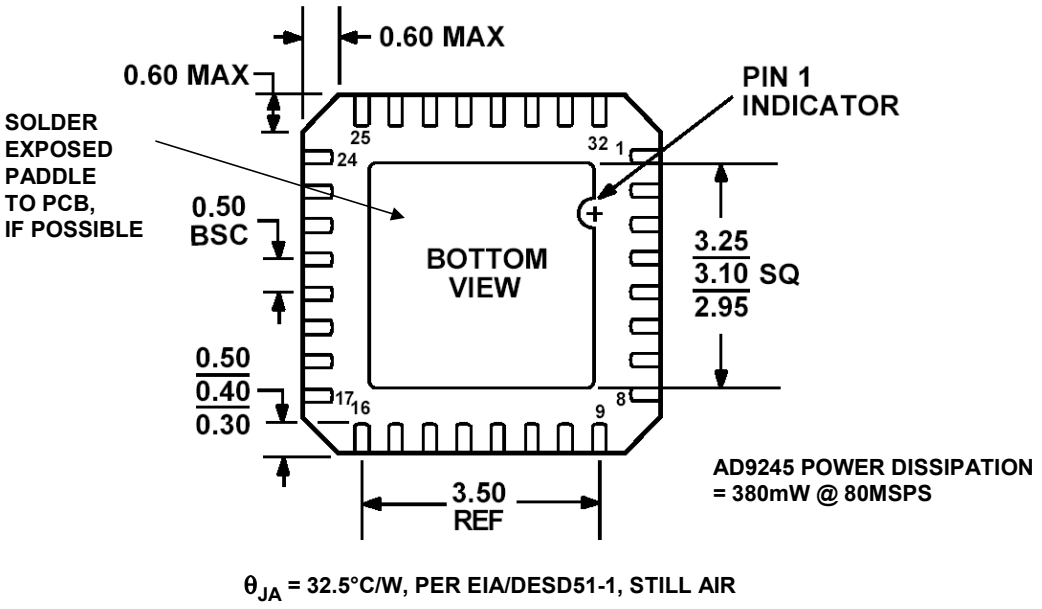


Figure 9.117: *AD9245 CP-32 Lead-Frame Chip-Scale Package (LFCSP), Bottom View*

The AD9430 is a high performance 12-bit, 170-/210-MSPS 3.3-V BiCMOS ADC. Two output modes are available: dual 105-MSPS demultiplexed CMOS outputs, or 210-MSPS LVDS outputs. Power dissipation as a function of sampling frequency is shown in Figure 9.118. Analog and digital supply currents are shown for CMOS and LVDS modes for an analog input frequency of 10.3 MHz. Note that in the LVDS mode and a sampling frequency of 210 MSPS, total supply current is approximately 455 mA—yielding a total power dissipation of 1.5 W.

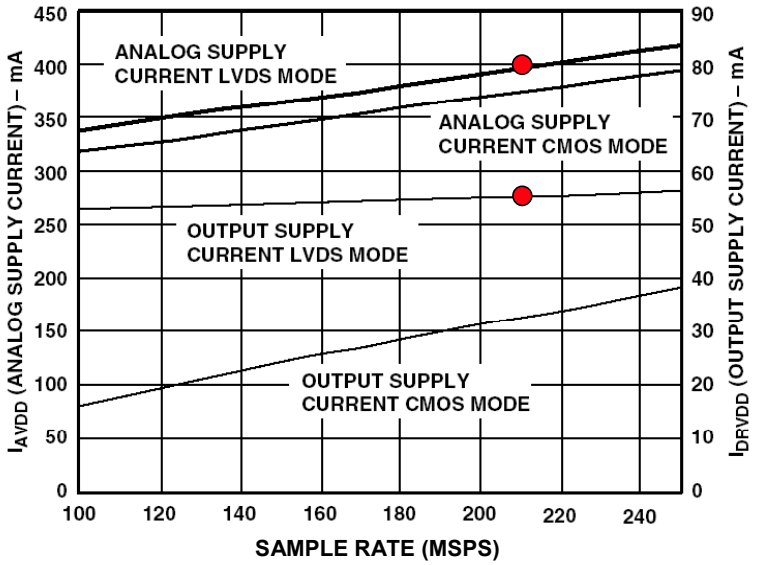


Figure 9.118: *AD9430 12-Bit 170-/210-MSPS ADC Supply Current vs.Sample Rate for 10.3-MHz Input*

The AD9430 is available in a 100-lead thin plastic quad flat package with an exposed pad (TQFP/EP) as shown in Figure 9.119. The conducive pad is connected to chip ground and should be soldered to the PC board ground plane. The θ_{JA} of the package when soldered to the ground plane is 25°C/W in still air. This places the junction 25°C × 1.5 = 37.5°C above the ambient temperature for 1.5 W of power dissipation. For a maximum operating temperature of +85°C, this places the junction at 85°C + 37.5°C = 122.5°C.

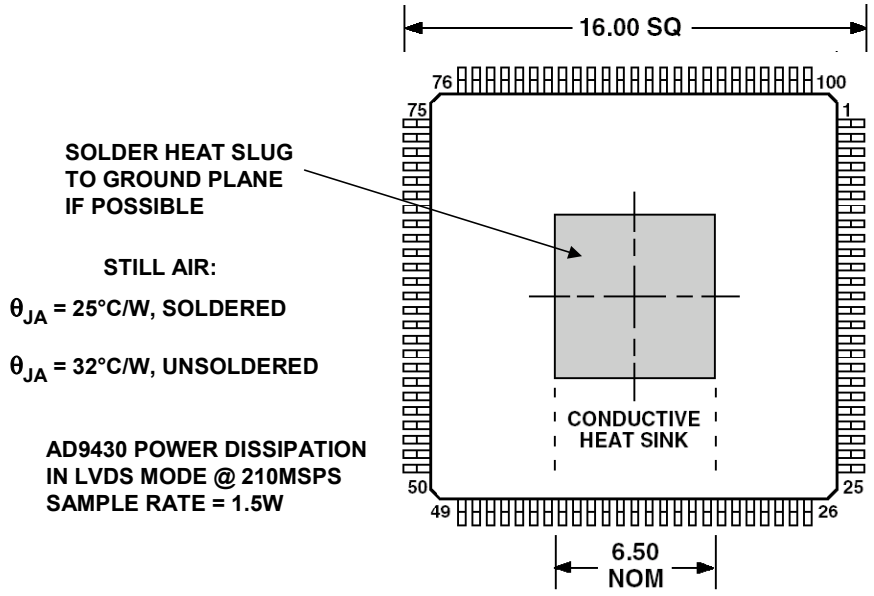


Figure 9.119: *AD9430 100-Lead e-PAD TQFP*

The AD6645 is a high performance 14-bit, 80-/105-MSPS ADC fabricated on a high speed complementary bipolar process (XFCB), and offers the highest SFDR (89 dBc) and SNR (75 dB) currently available in 2004. Although there is little variation in power as a function of sampling frequency, the maximum power dissipation of the device is 1.75 W. The package is a thermally enhanced 52-lead PowerQuad 4® with an exposed pad as shown in Figure 9.120.

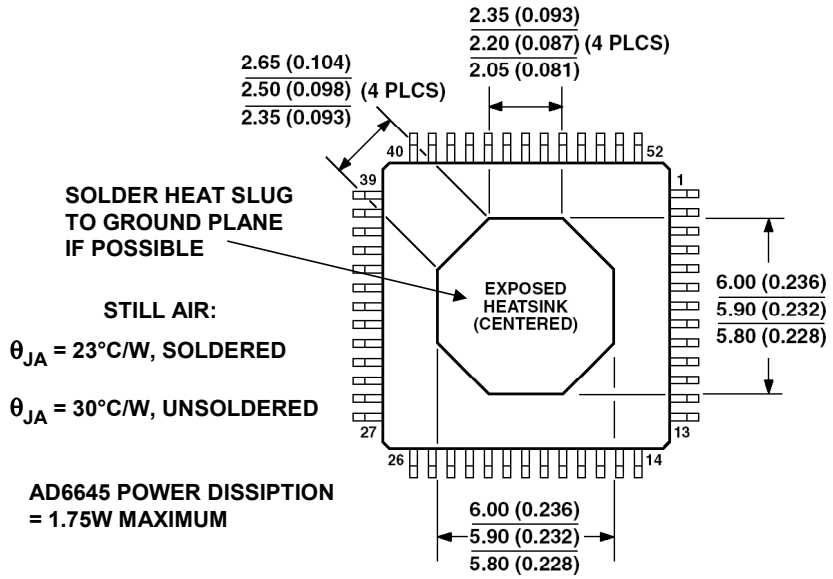


Figure 9.120:*AD6645 52-Lead Power-Quad 4 (LQFP_ED)*
(SQ-52) Thermally Enhanced Package, Bottom View

It is recommended that the exposed center heatsink be soldered to the PC board ground plane to reduce the package θ_{JA} to 23°C/W in still air. For 1.75 W of power dissipation, this places the junction temperature 23°C × 1.75 = 40.3°C above the ambient temperature. For a maximum operating temperature of +85°C, this places the junction at 85°C + 40.3°C = 125.3°C. The thermal resistance of the package can be reduced to 17°C/W with 200 LFPM airflow, thereby reducing the junction temperature to 30°C above the ambient, or 115°C for an operating ambient temperature of +85°C.

High speed CMOS DACs (such as the TxDAC® series) and DDS ICs (such as the AD985x series) also have clock-rate dependent power dissipation. For example, in the case of the AD9777 16-bit, 160-MSPS dual interpolating DAC, power dissipation is a function of clock rate, output frequency, and the enabling of the PLL and the modulation functions. Power dissipation on 3.3-V supplies can range from 380 mW (f_{DAC} = 100 MSPS, f_{OUT} = 1 MHz, no interpolation, no modulation) to 1.75 W (f_{DAC} = 400 MSPS, f_{DATA} = 50 MHz, $f_s/2$ modulation, PLL enabled). These and similar parts in the family are also offered in thermally enhanced packages with exposed pads for soldering to the PC board ground plane.

These discussions on the thermal application issues of op amps and data converters haven't dealt with the classic techniques of using clip-on (or bolt-on) type heat sinks. They also have not addressed the use of forced air cooling, generally considered only when tens of watts must be handled. These omissions are mainly because these approaches are seldom possible or practical with today's op amp and data converter packages.

The more general discussions within References 4-7 can be consulted for this and other supplementary information.

REFERENCES:
9.5 THERMAL MANAGEMENT

1. Data sheet for **AD8017 Dual High Output Current, High Speed Amplifier**, Analog Devices, Inc., http://www.analog.com

2. Data sheet for **AD8016 Low Power, High Output Current, xDSL Line Driver**, Analog Devices, Inc., http://www.analog.com/.

3. "Power Consideration Discussions," data sheet for **AD815 High Output Current Differential Driver**, Analog Devices, Inc., http://www.analog.com/.

4. Walt Jung, Walt Kester, "Thermal Management," portion of Section 8 within Walt Kester, Editor, **Practical Design Techniques for Power and Thermal Management**, Analog Devices, Inc., 1998, ISBN 0-916550-19-2.

5. General Catalog, **AAVID Thermal Technologies, Inc.**, One Kool Path, Laconia, NH, 03246, (603) 528-3400.

6. Seri Lee, "How to Select a Heat Sink," **Aavid Thermal Technologies**, http://www.aavid.com

7. Seri Lee, "Optimum Design and Selection of Heat Sinks," **11th IEEE SEMI-THERM™ Symposium**, 1995, http://www.aavid.com.

NOTES:

SECTION 9.6: EMI/RFI CONSIDERATIONS

James Bryant, Walt Jung, Walt Kester

Analog circuit performance is often affected adversely by high frequency signals from nearby electrical activity. And, equipment containing your analog circuitry may also adversely affect systems external to it. Reference 1 (page 4) describes this complementary transmission of undesirable high frequency signals from or into local equipment as per an IEC50 definition. These corresponding aspects of the broad arena of *electromagnetic compatibility*, better known as EMC, are:

- *It describes the ability of electrical and electronic systems to operate without interfering with other systems…*
- *It also describes the ability of such systems to operate as intended within a specified electromagnetic environment.*

So, complete EMC assurance would indicate that the equipment under design should neither produce spurious signals, nor should it be vulnerable to out-of-band external signals (i.e., those outside its intended frequency range). It is the latter class of EMC problem to which analog equipment most often falls prey. And, it is the graceful handling of these spurious signals that are emphasized within this section.

The externally produced electrical activity may generate noise, and is referred to either as electromagnetic interference (EMI), or radio frequency interference (RFI). In this section, we will refer to EMI in terms of both electromagnetic and radio frequency interference. One of the more challenging tasks of the analog designer is the control of equipment against undesired operation due to EMI. It is important to note that in this context, *EMI and or RFI is almost always detrimental*. Once given entrance into your equipment, it can and will degrade its operation, quite often considerably.

This section is oriented heavily towards minimizing undesirable analog circuit operation due to the *receipt* of EMI/RFI. Misbehavior of this sort is also known as EMI or RFI *susceptibility*, indicating a tendency towards anomalous equipment behavior when exposed to EMI/RFI. There is of course a complementary EMC issue, namely with regard to spurious *emissions*. However, since analog circuits typically involve fewer pulsed, high speed, high current signal edges that give rise to such spurious signals (compared to high speed logic, for example), this aspect of EMC isn't as heavily treated here. Nevertheless, the reader should bear in mind that it can be important, particularly if the analog circuitry is part of a mixed-signal environment along with high speed logic.

Since all of these various EMC design points can be critical, *the end-of-chapter references are strongly recommended for supplementary study*. Indeed, for a thorough, fully competent design with respect to EMI, RFI and EMC, the designer will need to become intimately acquainted with one or more of these references (see References 1- 6). As for the material following, it is best viewed as an introduction to this extremely broad but increasingly important topic.

EMI/RFI Mechanisms

To understand and properly control EMI and RFI, it is helpful to first segregate it into manageable portions. Thus it is useful to remember that when EMI/RFI problems do occur, they can be fundamentally broken down into a *Source*, a *Path*, and a *Receiver*. As a systems designer, you have under your direct control the receiver part of this landscape, and perhaps some portion of the path. But seldom will the designer have control over the actual source.

EMI Noise Sources

There are countless ways in which undesired noise can couple into an analog circuit to ruin its accuracy. Some of the many examples of these noise sources are listed in Figure 9.121.

- **EMI/RFI noise sources can couple from *anywhere***
- **Some common sources of externally generated noise:**
  - **Radio and TV Broadcasts**
  - **Mobile Radio Communications**
  - **Cellular Telephones**
  - **Vehicular Ignition**
  - **Lightning**
  - **Utility Power Lines**
  - **Electric Motors**
  - **Computers**
  - **Garage Door Openers**
  - **Telemetry Equipment**

Figure 9.121: *Some Common EMI Noise Sources*

Since little control is possible over these sources of EMI, the next best management tool one can exercise over them is to recognize and understand the possible paths by which they couple into the equipment under design.

EMI Coupling Paths

The EMI coupling paths are actually very few in terms of basic number. Three very general paths are by:

1. *Interference due to conduction (common-impedance)*
2. *Interference due to capacitive or inductive coupling (near-field interference)*
3. *Electromagnetic radiation (far-field interference)*

Noise Coupling Mechanisms

EMI energy may enter wherever there is an impedance mismatch or discontinuity in a system. In general this occurs at the interface where cables carrying sensitive analog signals are connected to PC boards, and through power supply leads. Improperly connected cables or poor supply filtering schemes are often perfect conduits for interference.

Conducted noise may also be encountered when two or more currents share a common path (impedance). This common path is often a high impedance "ground" connection. If two circuits share this path, noise currents from one will produce noise voltages in the other. Steps may be taken to identify potential sources of this interference (see References 1 and 2, plus section 2 of this chapter).

Figure 9.122 shows some of the general ways noise can enter a circuit from external sources.

- **Impedance mismatches and discontinuities**
- **Common-mode impedance mismatches → Differential Signals**
- **Capacitively Coupled (Electric Field Interference)**
  - **dV/dt → Mutual Capacitance → Noise Current**
    (Example: 1V/ns produces 1mA/pF)
- **Inductively Coupled (Magnetic Field)**
  - **di/dt → Mutual Inductance → Noise Voltage**
    (Example: 1mA/ns produces 1mV/nH)

Figure 9.122: *How EMI finds Paths into Equipment*

There is a capacitance between any two conductors separated by a dielectric (air and vacuum are dielectrics, as well as all solid or liquid insulators). If there is a change of voltage on one conductor there will be change of charge on the other, and a *displacement current* will flow in the dielectric. Where either the capacitance or the dV/dT is high, noise is easily coupled. For example, a 1-V/ns rate-of-change gives rise to displacement currents of 1 mA/pF.

If changing magnetic flux from current flowing in one circuit couples into another circuit, it will induce an emf in the second circuit. Such *mutual inductance* can be a troublesome source of noise coupling from circuits with high values of dI/dT. As an example, a mutual inductance of 1 nH and a changing current of 1 A/ns will induce an emf of 1 V.

Reducing Common-Impedance Noise

Steps to be taken to eliminate or reduce noise due to the conduction path sharing of impedances, or *common-impedance noise* are outlined in Figure 9.123.

- **Common-impedance noise**
  - **Decouple op amp power leads at LF and HF**
  - **Reduce common-impedance**
  - **Eliminate shared paths**
- **Techniques**
  - **Low impedance electrolytic (LF) and local low inductance (HF) bypasses**
  - **Use ground and power planes**
  - **Optimize system design**

Figure 9.123: *Some Solutions to Common-Impedance Noise*

These methods should be applied in conjunction with all of the related techniques discussed earlier within section 2 of this chapter.

Power supply rails feeding several circuits are good common-impedance examples. Real world power sources may exhibit low output impedance, or may they not—especially over frequency. Furthermore, PCB traces used to distribute power are both inductive and resistive, and may also form a ground loop. The use of power and ground planes also reduces the power distribution impedance. These dedicated conductor layers in a PCB are continuous (ideally, that is) and as such, offer the lowest practical resistance and inductance.

In some applications where low-level signals encounter high levels of common-impedance noise it will not be possible to prevent interference and the system architecture may need to be changed. Possible changes include:

1. *Transmitting signals in differential form*
2. *Amplifying signals to higher levels for improved S/N*
3. *Converting signals into currents for transmission*
4. *Converting signals directly into digital form*

Noise Induced by Near-Field Interference

Crosstalk is the second most common form of interference. In the vicinity of the noise source, i.e., near-field, interference is not transmitted as an electromagnetic wave, and the term crosstalk may apply to either inductively or capacitively coupled signals.

Reducing Capacitance-Coupled Noise

Capacitively-coupled noise may be reduced by reducing the coupling capacity (by increasing conductor separation), but is most easily cured by shielding. A conductive and grounded shield (known as a *Faraday shield*) between the signal source and the affected node will eliminate this noise, by routing the displacement current directly to ground.

With the use of such shields, it is important to note that it is always *essential* that a Faraday shield be grounded. A floating or open-circuit shield almost invariably increases

capacitively-coupled noise. For a brief review of this shielding, consult Section 2 of this chapter again, and see References 2 and 3 at the end of this section.

Methods to eliminate capacitance-coupled interference are summarized in Figure 9.124.

- **Reduce Level of High dV/dt Noise Sources**
- **Use Proper Grounding Schemes for Cable Shields**
- **Reduce Stray Capacitance**
  - **Equalize Input Lead Lengths**
  - **Keep Traces Short**
  - **Use Signal-Ground Signal-Routing Schemes**
- **Use Grounded Conductive Faraday Shields to Protect Against Electric Fields**

Figure 9.124: *Methods to Reduce Capacitance-Coupled Noise*

Reducing Magnetically-Coupled Noise

Methods to eliminate interference caused by magnetic fields are summarized in Figure 9.125.

- **Careful Routing of Wiring**
- **Use Conductive Screens for HF Magnetic Shields**
- **Use High Permeability Shields for LF Magnetic Fields (mu-Metal)**
- **Reduce Loop Area of Receiver**
  - **Twisted Pair Wiring**
  - **Physical Wire Placement**
  - **Orientation of Circuit to Interference**
- **Reduce Noise Sources**
  - **Twisted Pair Wiring**
  - **Driven Shields**

Figure 9.125: *Methods to Reduce Magnetically-Coupled Noise*

To illustrate the effect of magnetically-coupled noise, consider a circuit with a closed-loop area of A cm^2 operating in a magnetic field with an rms flux density value of B gauss. The noise voltage V_n induced in this circuit can be expressed by the following equation:

$$V_n = 2\,\pi\,f\,B\,A\,\cos\theta \times 10^{-8}\ V \qquad \text{Eq. 9.12}$$

In this equation, f represents the frequency of the magnetic field, and θ represents the angle of the magnetic field B to the circuit with loop area A. Magnetic field coupling can be reduced by reducing the circuit loop area, the magnetic field intensity, or the angle of

incidence. Reducing circuit loop area requires arranging the circuit conductors closer together. Twisting the conductors together reduces the loop net area. This has the effect of canceling magnetic field pickup, because the sum of positive and negative incremental loop areas is ideally equal to zero. Reducing the magnetic field directly may be difficult. However, since magnetic field intensity is inversely proportional to the cube of the distance from the source, physically moving the affected circuit away from the magnetic field has a very great effect in reducing the induced noise voltage. Finally, if the circuit is placed perpendicular to the magnetic field, pickup is minimized. If the circuit's conductors are in parallel to the magnetic field the induced noise is maximized because the angle of incidence is zero.

There are also techniques that can be used to reduce the amount of magnetic-field interference, *at its source*. In the previous paragraph, the conductors of the receiver circuit were twisted together, to cancel the induced magnetic field along the wires. The same principle can be used on the source wiring. If the source of the magnetic field is large currents flowing through nearby conductors, these wires can be twisted together to reduce the net magnetic field.

Shields and cans are not nearly as effective against magnetic fields as against electric fields, but can be useful on occasion. At low frequencies magnetic shields using high-permeability material such as Mu-metal can provide modest attenuation of magnetic fields. At high frequencies simple conductive shields are quite effective provided that the thickness of the shield is greater than the skin depth of the conductor used (at the frequency involved). Note—copper skin depth is $6.6/\sqrt{f}$ cm, with f in Hz.

Passive Components: Your Arsenal Against EMI

Passive components, such as resistors, capacitors, and inductors, are powerful tools for reducing externally induced interference when used properly.

Simple RC networks make efficient and inexpensive one-pole, low-pass filters. Incoming noise is converted to heat and dissipated in the resistor. But note that a fixed resistor does produce thermal noise of its own. Also, when used in the input circuit of an op amp or in-amp, such resistor(s) can generate input-bias-current induced offset voltage. While matching the two resistors will minimize the dc offset, the noise will remain. Figure 9.126 summarizes some popular low-pass filters for minimizing EMI.

In applications where signal and return conductors aren't well-coupled magnetically, a common-mode (CM) choke can be used to increase their mutual inductance. Note that these comments apply mostly to in-amps, which naturally receive a balanced input signal (whereas op amps are inherently unbalanced inputs—unless one constructs an in-amp with them). A CM choke can be simply constructed by winding several turns of the differential signal conductors together through a high-permeability (> 2000) ferrite bead. The magnetic properties of the ferrite allow differential-mode currents to pass unimpeded while suppressing CM currents.

LP Filter Type	ADVANTAGE	DISADVANTAGE
RC Section	Simple Inexpensive	Resistor Thermal Noise I_B x R Drop → Offset Single-Pole Cutoff
LC Section (Bifilar)	Very Low Noise at LF Very Low IR Drop Inexpensive Two-Pole Cutoff	Medium Complexity Nonlinear Core Effects Possible
π Section (C-L-C)	Very Low Noise at LF Very Low IR Drop Pre-packaged Filters Multiple-Pole Cutoff	Most Complex Nonlinear Core Effects Possible Expensive

Figure 9.126: *Using Passive Components Within Filters to Combat EMI*

Capacitors can also be used before and after the choke, to provide additional CM and differential-mode filtering, respectively. Such a CM choke is cheap and produces very low thermal noise and bias current-induced offsets, due to the wire's low dc resistance. However, there is a field around the core. A metallic shield surrounding the core may be necessary to prevent coupling with other circuits. Also, note that high-current levels should be avoided in the core as they may saturate the ferrite.

The third method for passive filtering takes the form of packaged π-networks (C-L-C). These packaged filters are completely self-contained and include feedthrough capacitors at the input and the output as well as a shield to prevent the inductor's magnetic field from radiating noise. These more expensive networks offer high levels of attenuation and wide operating frequency ranges, but the filters must be selected so that for the operating current levels involved the ferrite doesn’t saturate.

Reducing System Susceptibility to EMI

The general examples discussed above and the techniques illustrated earlier in this section outline the procedures that can be used to reduce or eliminate EMI/RFI. Considered on a *system* basis, a summary of possible measures is given in Figure 9.127.

Other examples of filtering techniques useful against EMI are illustrated later in this section, under "Reducing RFI rectification within op amp and in-amp circuits".

The section immediately below further details shielding principles.

- **Always Assume That Interference Exists!**
- **Use Conducting Enclosures Against Electric and HF Magnetic Fields**
- **Use mu-Metal Enclosures Against LF Magnetic Fields**
- **Implement Cable Shields Effectively**
- **Use Feedthrough Capacitors and Packaged PI Filters**

Figure 9.127: *Reducing System EMI/RFI Susceptibility*

A Review of Shielding Concepts

The concepts of shielding effectiveness presented next are background material. Interested readers should consult References 4-9 cited at the end of the section for more detailed information.

Applying the concepts of shielding effectively requires an understanding of the source of the interference, the environment surrounding the source, and the distance between the source and point of observation (the receiver). If the circuit is operating close to the source (in the *near*, or induction-field), then the field characteristics are determined by the source. If the circuit is remotely located (in the *far*, or radiation-field), then the field characteristics are determined by the transmission medium.

A circuit operates in a near-field if its distance from the source of the interference is less than the wavelength (λ) of the interference divided by 2π, or $\lambda/2\pi$. If the distance between the circuit and the source of the interference is larger than this quantity, then the circuit operates in the far field. For instance, the interference caused by a 1-ns pulse edge has an upper bandwidth of approximately 350 MHz. The wavelength of a 350-MHz signal is approximately 32 inches (the speed of light is approximately 12"/ns). Dividing the wavelength by 2π yields a distance of approximately 5 inches, the boundary between near- and far-field. If a circuit is within 5 inches of a 350-MHz interference source, then the circuit operates in the near-field of the interference. If the distance is greater than 5 inches, the circuit operates in the far-field of the interference.

Regardless of the type of interference, there is a characteristic impedance associated with it. The characteristic, or wave impedance of a field is determined by the ratio of its electric (or E-) field to its magnetic (or H-) field. In the far field, the ratio of the electric field to the magnetic field is the characteristic (wave impedance) of free space, given by $Z_O = 377\ \Omega$. In the near field, the wave-impedance is determined by the nature of the interference and its distance from the source. If the interference source is high-current and low-voltage (for example, a loop antenna or a power-line transformer), the field is predominately magnetic and exhibits a wave impedance which is less than 377 Ω. If the source is low-current and high-voltage (for example, a rod antenna or a high-speed digital switching circuit), then the field is predominately electric and exhibits a wave impedance which is greater than 377 Ω.

Conductive enclosures can be used to shield sensitive circuits from the effects of these external fields. These materials present an *impedance mismatch* to the incident interference, because the impedance of the shield is lower than the wave impedance of the incident field. The effectiveness of the conductive shield depends on two things: First is the loss due to the *reflection* of the incident wave off the shielding material. Second is the loss due to the *absorption* of the transmitted wave *within* the shielding material. The amount of reflection loss depends upon the type of interference and its wave impedance. The amount of absorption loss, however, is independent of the type of interference. It is the same for near- and far-field radiation, as well as for electric or magnetic fields.

Reflection loss at the interface between two media depends on the difference in the characteristic impedances of the two media. For electric fields, reflection loss depends on the frequency of the interference and the shielding material. This loss can be expressed in dB, and is given by:

$$R_e(\text{dB}) = 322 + 10\log_{10}\left[\frac{\sigma_r}{\mu_r f^3 r^2}\right] \qquad \text{Eq. 9.13}$$

where σ_r = relative conductivity of the shielding material, in Siemens per meter;
μ_r = relative permeability of the shielding material, in Henries per meter;
f = frequency of the interference, and
r = distance from source of the interference, in meters

For magnetic fields, the loss depends also on the shielding material and the frequency of the interference. Reflection loss for magnetic fields is given by:

$$R_m(\text{dB}) = 14.6 + 10\log_{10}\left[\frac{f r^2 \sigma_r}{\mu_r}\right] \qquad \text{Eq. 9.14}$$

and, for plane waves ($r > \lambda/2\pi$), the reflection loss is given by:

$$R_{pw}(\text{dB}) = 168 + 10\log_{10}\left[\frac{\sigma_r}{\mu_r f}\right] \qquad \text{Eq. 9.15}$$

Absorption is the second loss mechanism in shielding materials. Wave attenuation due to absorption is given by:

$$A(\text{dB}) = 3.34t\sqrt{\sigma_r \mu_r f} \qquad \text{Eq. 9.16}$$

where t = thickness of the shield material, in inches. This expression is valid for plane waves, electric and magnetic fields. Since the intensity of a transmitted field decreases exponentially relative to the thickness of the shielding material, the absorption loss in a shield one skin-depth (δ) thick is 9 dB. Since absorption loss is proportional to thickness and inversely proportional to skin depth, increasing the thickness of the shielding material improves shielding effectiveness at high frequencies.

Reflection loss for plane waves in the far field decreases with increasing frequency because the shield impedance, Z_s, increases with frequency. Absorption loss, on the other hand, increases with frequency because skin depth decreases. For electric fields and plane waves, the primary shielding mechanism is reflection loss, and at high frequencies, the mechanism is absorption loss.

Thus for high-frequency interference signals, lightweight, easily worked high conductivity materials such as copper or aluminum can provide adequate shielding. At low frequencies however, both reflection and absorption loss to magnetic fields is low. It is thus very difficult to shield circuits from low-frequency magnetic fields. In these applications, high-permeability materials that exhibit low-reluctance provide the best protection. These low-reluctance materials provide a magnetic shunt path that diverts the magnetic field away from the protected circuit.

To summarize the characteristics of metallic materials commonly used for shielded purposes: Use high conductivity metals for HF interference, and high permeability metals for LF interference.

A properly shielded enclosure is very effective at preventing external interference from disrupting its contents as well as confining any internally-generated interference. However, in the real world, openings in the shield are often required to accommodate adjustment knobs, switches, connectors, or to provide ventilation. Unfortunately, these openings may compromise shielding effectiveness by providing paths for high-frequency interference to enter the instrument.

The longest dimension (not the total area) of an opening is used to evaluate the ability of external fields to enter the enclosure, because the openings behave as slot antennas. Equation Eq. 9.17 can be used to calculate the shielding effectiveness, or the susceptibility to EMI leakage or penetration, of an opening in an enclosure:

$$\text{Shielding Effectiveness (dB)} = 20\log_{10}\left(\frac{\lambda}{2\cdot L}\right) \qquad \text{Eq. 9.17}$$

where λ = wavelength of the interference and
L = maximum dimension of the opening

Maximum radiation of EMI through an opening occurs when the longest dimension of the opening is equal to one half-wavelength of the interference frequency (0-dB shielding effectiveness). A rule-of-thumb is to keep the longest dimension less than 1/20 wavelength of the interference signal, as this provides 20-dB shielding effectiveness. Furthermore, a few small openings on each side of an enclosure is preferred over many openings on one side. This is because the openings on different sides radiate energy in different directions, and as a result, shielding effectiveness is not compromised. If openings and seams cannot be avoided, then conductive gaskets, screens, and paints alone or in combination should be used judiciously to limit the longest dimension of any opening to less than 1/20 wavelength. Any cables, wires, connectors, indicators, or control shafts penetrating the enclosure should have circumferential metallic shields

physically bonded to the enclosure at the point of entry. In those applications where unshielded cables/wires are used, then filters are recommended at the shield entry point.

General Points on Cables and Shields

Although covered in detail elsewhere, it is worth noting that the improper use of cables and their shields can be a significant contributor to both radiated and conducted interference. Rather than developing an entire treatise on these issues, the interested reader should consult References 2, 3, 5, and 6 for background.

As shown in Figure 9.128, proper cable/enclosure shielding confines sensitive circuitry and signals *entirely within the shield*, with no compromise to shielding effectiveness.

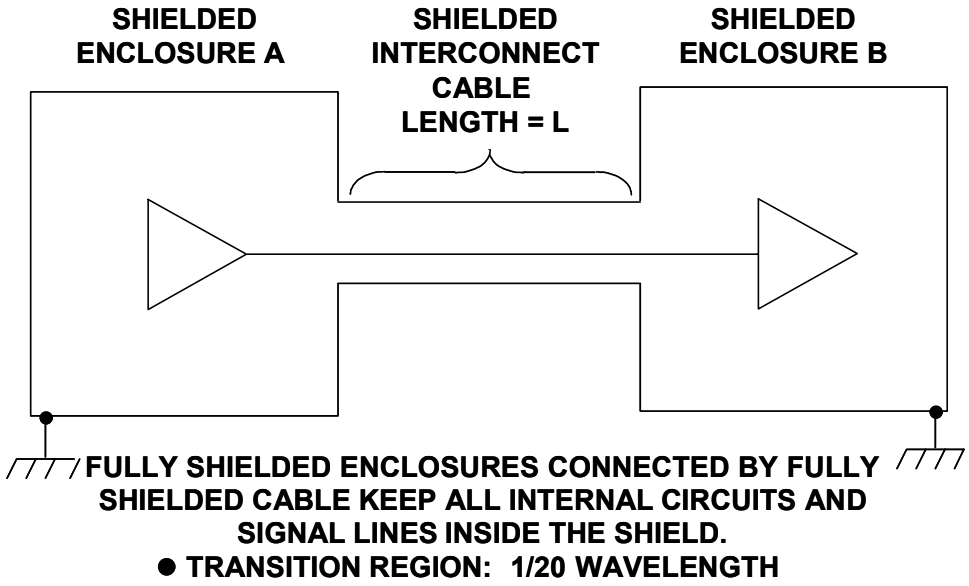


Figure 9.128: *Shielded Interconnect Cables Are Either Electrically Long or Short, Depending Upon the Operating Frequency*

As can be noted by this diagram, the enclosures and the shield must be grounded properly, otherwise they can act as an antenna, thereby making the radiated and conducted interference problem worse (rather than better).

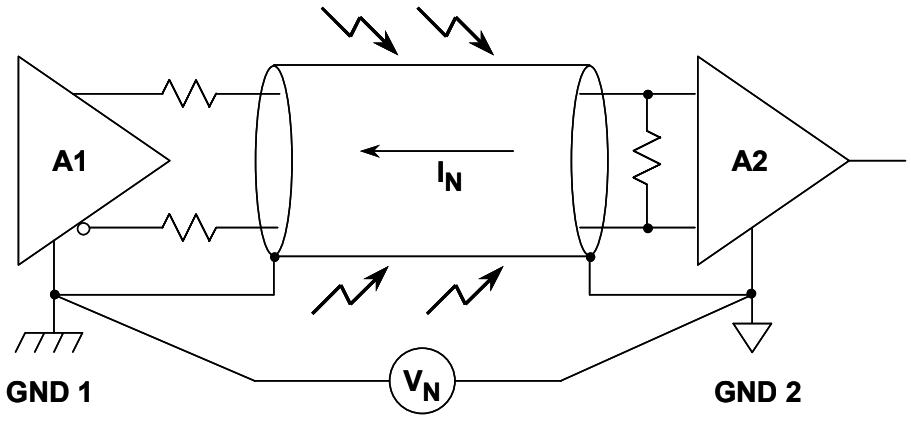
Depending on the type of interference (pickup/radiated, low/high frequency), proper cable shielding is implemented differently and is very dependent on the length of the cable. The first step is to determine whether the length of the cable is *electrically short* or *electrically long* at the frequency of concern. A cable is considered electrically short if the length of the cable is less than 1/20 wavelength of the highest frequency of the interference. Otherwise it is considered to be electrically long.

For example, at 50/60 Hz, an electrically short cable is any cable length less than 150 miles, where the primary coupling mechanism for these low frequency electric fields is capacitive. As such, for any cable length less than 150 miles, the amplitude of the interference will be the same over the entire length of the cable.

In applications where the length of the cable is electrically long, or protection against high-frequency interference is required, then the preferred method is to connect the cable shield to low-impedance points, *at both ends*. As will be seen shortly, this can be a direct connection at the driving end, and a capacitive connection at the receiver. If left ungrounded, unterminated transmission lines effects can cause reflections and standing waves along the cable. At frequencies of 10 MHz and above, circumferential (360°) shield bonds and metal connectors are required to main low-impedance connections to ground.

In summary, for protection against low-frequency (<1 MHz), electric-field interference, grounding the shield at one end is acceptable. For high-frequency interference (>1 MHz), the preferred method is grounding the shield at both ends, using 360° circumferential bonds between the shield and the connector, and maintaining metal-to-metal continuity between the connectors and the enclosure.

However in practice, there is a caveat involved with directly grounding the shield at both ends. When this is done, it creates a low frequency ground loop, shown in Figure 9.129.



- **V_N Causes Current in Shield (Usually 50/60Hz)**
- **Differential Error Voltage is Produced at Input of A2 Unless:**
  - **A1 Output is Perfectly Balanced and**
  - **A2 Input is Perfectly Balanced and**
  - **Cable is Perfectly Balanced**

Figure 9.129: *Ground Loops in Shielded Twisted Pair Cable Can Cause Errors*

Whenever two systems A1 and A2 are remote from each other, there is usually a difference in the ground potentials at each system, i.e., V_N. The frequency of this potential difference is generally the line frequency (50 or 60 Hz) and multiples thereof. But, if the shield is directly grounded at both ends as shown, noise current I_N flows in the shield. In a perfectly balanced system, the common-mode rejection of the system is infinite, and this current flow produces no differential error at the receiver A2. However, perfect balance is never achieved in the driver, its impedance, the cable, or the receiver, so a certain portion of the shield current will appear as a differential noise signal, at the input of A2. The following illustrate correct shield grounding for various examples.

As noted above, cable shields are subject to both low and high frequency interference. Good design practice requires that the shield be grounded at both ends if the cable is electrically long to the interference frequency, as is usually the case with RF interference.

Figure 9.130 shows a remote passive RTD sensor connected to a bridge and conditioning circuit by a shielded cable. The proper grounding method is shown in the upper part of the figure, where the shield is grounded at the receiving end.

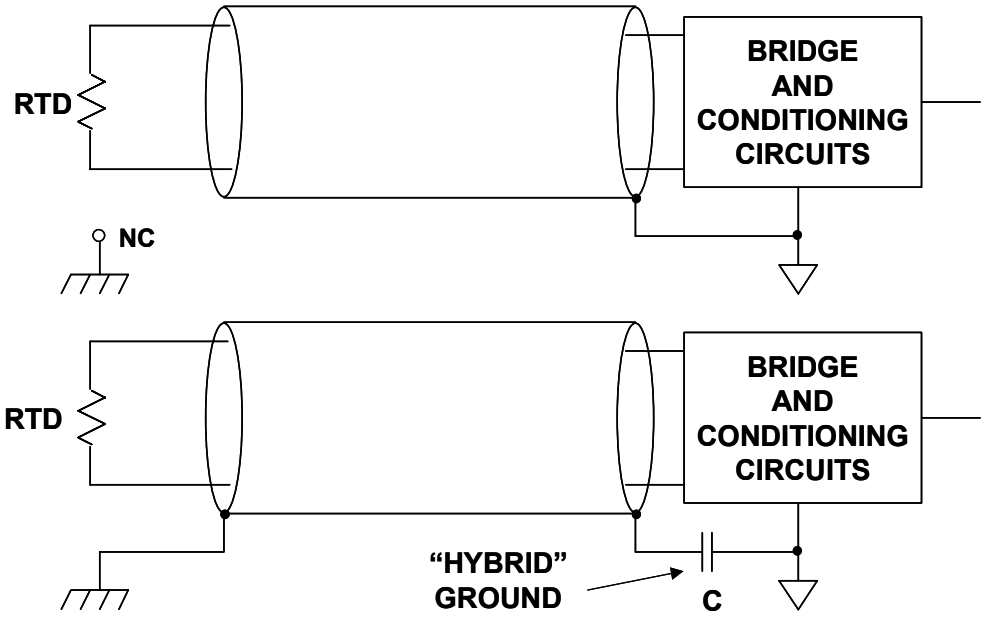


Figure 9.130: *Hybrid Grounding of Shielded Cable With Passive Sensor*

However, safety considerations may require that the remote end of the shield also be grounded. If this is the case, the receiving end can be grounded with a low inductance ceramic capacitor (0.01 μF to 0.1 μF), still providing high frequency grounding. The capacitor acts as a ground to RF signals on the shield but blocks low frequency line current to flow in the shield. This technique is often referred to as a *hybrid ground*.

A case of an active remote sensor and/or other electronics is shown Figure 9.131. In both of the two situations, a hybrid ground is also appropriate, either for the balanced (upper) or the single-ended (lower) driver case. In both instances the capacitor "C" breaks the low frequency ground loop, providing effective RF grounding of the shielded cable at the A2 receiving end at the right side of the diagram.

There are also some more subtle points that should be made with regard to the source termination resistances used, R_S. In both the balanced as well as the single-ended drive cases, the driving signal seen on the balanced line originates from a net impedance of R_S, which is split between the two twisted pair legs as twice $R_S/2$. In the upper case of a fully differential drive, this is straightforward, with an $R_S/2$ valued resistor connected in series with the complementary outputs from A1.

In the bottom case of the single-ended driver, note that there are still two $R_S/2$ resistors used, one in series with both legs. Here the grounded dummy return leg resistor provides an impedance-balanced ground connection drive to the differential line, aiding in overall system noise immunity. Note that this implementation is only useful for those applications with a balanced receiver at A2, as shown.

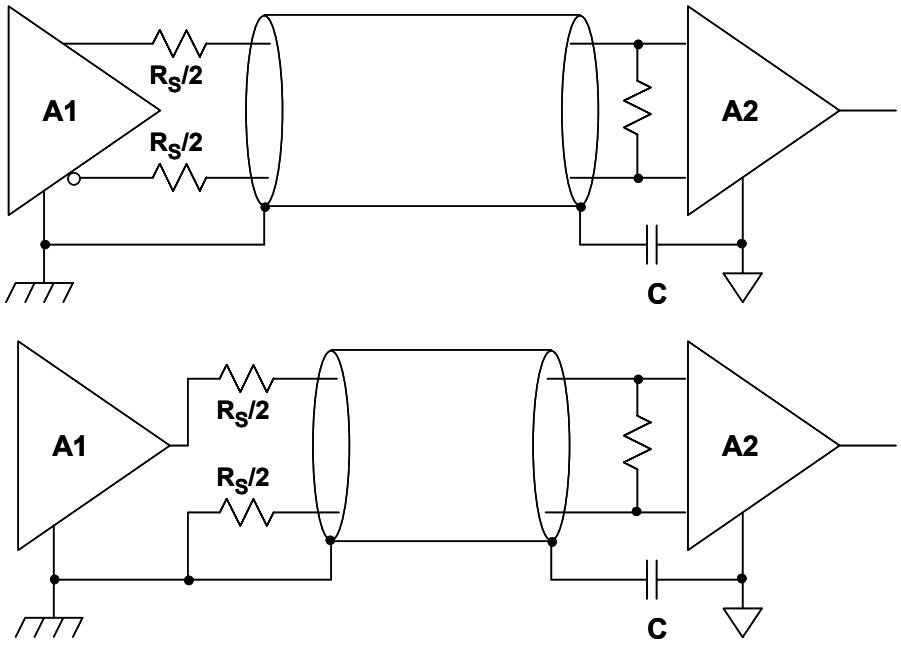


Figure 9.131: *Impedance-Balanced Drive of Balanced Shielded Cable Aids Noise-Immunity With Either Balanced or Single-Ended Source Signals*

Coaxial cables are different from shielded twisted pair cables in that the signal return current path is through the shield. For this reason, the ideal situation is to ground the shield at the driving end and allow the shield to float at the differential receiver (A2) as shown in the upper portion of Figure 9.132. For this technique to work, however, the receiver must be a differential type with good high frequency CM rejection.

However, the receiver may be a single-ended type, such as typical of a standard single op amp type circuit. This is true for the bottom example of Figure 9.132, so there is no choice but to ground the coaxial cable shield at both ends for this case.

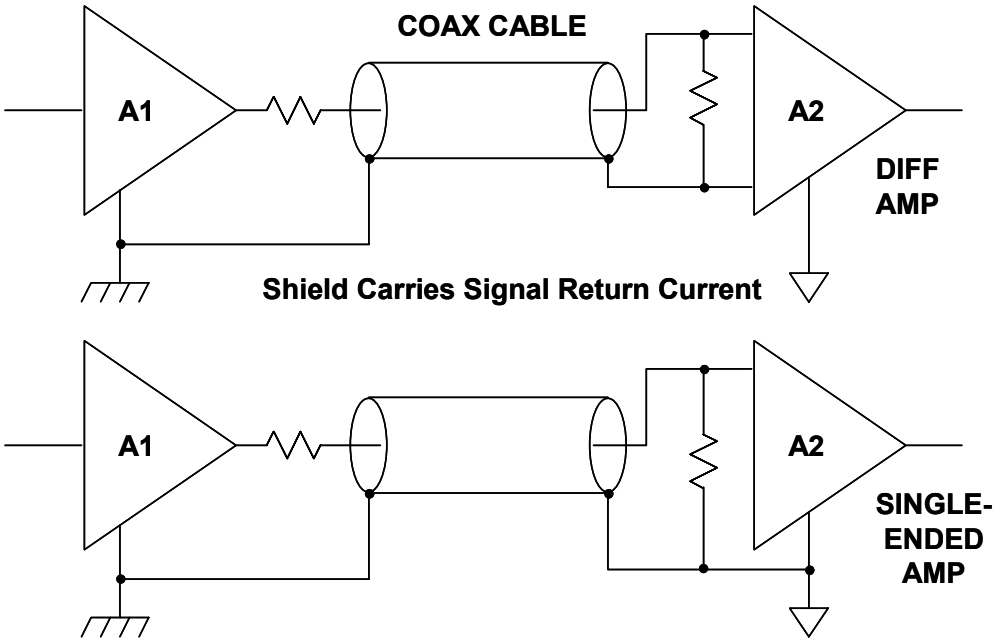


Figure 9.132: *Coaxial Cables Can Use Either Balanced or Single-Ended Receivers*

Input-Stage RFI Rectification Sensitivity

A well-known but poorly understood phenomenon in analog integrated circuits is *RFI rectification*, specifically as it occurs in op amps and in-amps. While amplifying very small signals these devices can rectify large-amplitude, out-of-band HF signals, i.e., RFI. As a result, dc errors appear at the output in addition to the desired signal. The undesired HF signals can enter sensitive analog circuits by various means. Conductors leading into and out of the circuit provide a path for interference coupling into a circuit. These conductors pick up noise through capacitive, inductive, or radiation coupling, as discussed earlier. The spurious signals appear at the amplifier inputs, along with the desired signal. The spurious signals can be several tens of mV in amplitude however, which causes problems. Simply stated, it cannot be assumed that a sensitive, low-bandwidth dc amplifier will always reject out-of-band spurious signals. While this would be the case for a simple linear low pass filter, op amp and in-amp devices actually rectify high-level HF signals, leading to non-linearities and anomalous offsets. Methods of analysis for as well as the prevention of RFI rectification are discussed in this section.

Background: Op Amp and In-Amp RFI Rectification Sensitivity Tests

Just about all in-amp and op amp input stages use emitter-coupled BJT or source-coupled FET differential pairs of some type. Depending on the device operating current, the interfering frequency and its relative amplitude, these differential pairs can behave as high-frequency detectors. As will be shown, the detection process produces spectral components at the harmonics of the interference, as well at dc! It is the detected dc component of the interference that shifts amplifier bias levels, leading to inaccuracies.

The effect of RFI rectification within op amps and in-amps can be evaluated with relatively simple test circuits, as described for the *RFI Rectification Test Configuration* (see page 1-38 of Reference 10). In these tests, an op amp or in-amp is configured for a gain of –100 (op amp), or 100 (in-amp), with dc output measured after a 100-Hz low-pass filter, preventing interference from other signals. A 100-MHz, 20-mV_{p-p} signal is the test stimulus, chosen to be well above test device frequency limits. In operation, the test evaluates dc output shift observed under stimulus presence. While an ideal dc shift for this measurement would be zero, the actual dc shift of a given part indicates the relative RFI rectification sensitivity. Devices using both BJT and FET technologies can be tested by this method, as can devices operating at either low or high supply current levels.

In the original op amp test device set of Reference 10, some FET-input devices (OP80, OP42, OP249 and AD845) exhibited no observable shift in their output voltages, while several others showed shifts of less than 10 μV referred to the input. Of the BJT-input op amps, the amount of shift decreased with increasing device supply current. Only two devices showed no observable output voltage shift (AD797 and AD827), while others showed shifts of less than 10 μV referred to the input (OP200 and OP297). For other op amps, it is to be expected that similar patterns would be shown under such testing.

From these tests, some generalizations on RFI rectification can be made. First, device susceptibility appears to be inversely proportional to supply current; that is, devices biased at low quiescent supply currents exhibit greatest output voltage shift. Second, ICs with FET-input stages appeared to be less susceptible to rectification than those with BJTs. Note that these points are independent of whether the device is an op amp or an in-amp. In practice this means that the lower power op amps *or* in-amps will tend to be more susceptible to RFI rectification effects. And, FET-input op amps (or in-amps) will tend to be *less* susceptible to RFI, especially those operating at higher currents.

Based on these data and from the fundamental differences between BJTs and FETs, we can summarize what we know. Bipolar transistor action is controlled by a forward-biased p-n junction (the base-emitter junction) whose I-V characteristic is exponential and quite nonlinear. FET behavior, on the other hand, is controlled by voltages applied to a reverse-biased p-n junction diode (the gate-source junction). The I-V characteristic of FETs is a square-law, and thus it is inherently more linear than that of BJTs.

For the case of the lower supply current devices, transistors in the circuit are biased well below their peak f_T collector currents. Although the ICs may be constructed on processes whose device f_ts can reach hundreds of MHz, charge transit times increase, when transistors are operated at low current levels. The impedance levels used also make RFI rectification in these devices worse. In low-power op amps, impedances are on the order of hundreds to thousands of kΩs, whereas in moderate supply-current designs impedances might be no more than just a few kΩ. Combined, these factors tend to degrade a low-power device's RFI rectification sensitivity.

Figure 9.133 summarizes these general observations on RFI rectification sensitivity, and is applicable to both op amps and in-amps.

- **BJT input devices *rectify readily***
  - **Forward-biased B-E junction**
  - **Exponential I-V Transfer Characteristic**
- **FET input devices *less sensitive* to rectifying**
  - **Reversed-biased p-n junction**
  - **Square-law I-V Transfer Characteristic**
- **Low I_{supply} devices versus High I_{supply} devices**
  - **Low I_{supply} $\Rightarrow$ *Higher* rectification sensitivity**
  - **High I_{supply} $\Rightarrow$ *Lower* rectification sensitivity**

Figure 9.133: *Some General Observations on Op Amp and In-Amp Input Stage RFI Rectification Sensitivity*

An Analytical Approach: BJT RFI Rectification

While lab experiments can demonstrate that BJT-input devices exhibit greater RFI rectification sensitivity than comparable devices with FET inputs, a more analytical approach can also be taken to explain this phenomenon.

RF circuit designers have long known that p-n junction diodes are efficient rectifiers because of their nonlinear I-V characteristics. A spectral analysis of a BJT transistor current output for a HF sinewave input reveals that, as the device is biased closer to its "knee," nonlinearity increases. This, in turn, makes its use as a detector more efficient. This is especially true in low-power op amps, where input transistors are biased at very low collector currents.

A rectification analysis for the collector current of a BJT has been presented in Reference 10, and will not be repeated here except for the important conclusions. These results reveal that the original quadratic second-order term can be simplified into a frequency-dependent term, $\Delta i_C(AC)$, at twice the input frequency and a dc term, $\Delta i_C(DC)$. The latter component can be expressed as noted in Eq. 9.18, the final form for the rectified dc term:

$$\Delta i_C(DC) = \left(\frac{V_X}{V_T}\right)^2 \bullet \frac{I_C}{4} \qquad \text{Eq. 9.18}$$

This expression shows that the dc component of the second-order term is directly proportional to the *square* of the HF noise amplitude V_X, and, also, to I_C, the quiescent collector current of the transistor. To illustrate this point on rectification, note that the change in dc collector current of a bipolar transistor operating at an I_C of 1 mA with a spurious 10-mV_{peak} high-frequency signal impinging upon it will be about 38 µA.

Reducing the amount of rectified collector current is a matter of reducing the quiescent current, or the magnitude of the interference. Since the op amp and in-amp input stages seldom provide adjustable quiescent collector currents, reducing the level of interfering noise V_X is by far the best (and almost always the only) solution. For example, reducing the amplitude of the interference by a factor of 2, down to 5 mV_{peak} produces a net 4 to 1

reduction in the rectified collector current. Obviously, this illustrates the importance of keeping spurious HF signals away from RFI sensitive amplifier inputs.

An Analytical Approach: FET RFI Rectification

A rectification analysis for the drain current of a JFET has also been presented in Reference 10, and isn't repeated here. A similar approach was used for the rectification analysis of a FET's drain current as a function of a small voltage V_X, applied to its gate. The results of evaluating the second-order rectified term for the FET's drain current are summarized in Eq. 9.19. Like the BJT, an FET's second-order term has an ac and a dc component. The simplified expression for the dc term of the rectified drain current is given here, where the rectified dc drain current is directly proportional to the square of the amplitude of V_X, the spurious signal. However, Eq. 9.19 also reveals a very important difference between the *degree* of the rectification produced by FETs relative to BJTs.

$$\Delta i_D(DC) = \left(\frac{V_X}{V_P}\right)^2 \bullet \frac{I_{DSS}}{2} \qquad \text{Eq. 9.19}$$

Whereas in a BJT the change in collector current has a direct relationship to its quiescent collector current level, the change in a JFET's drain current is proportional to its drain current at zero gate-source voltage, I_{DSS}, and inversely proportional to the square of its channel pinch-off voltage, V_P—parameters that are geometry and process dependent. Typically, JFETs used in the input stages of in-amps and op amps are biased with their quiescent current of ~$0.5 \cdot I_{DSS}$. Therefore, the change in a JFET's drain current is independent of its quiescent drain current; hence, independent of the operating point.

A quantitative comparison of second-order rectified dc terms between BJTs and FETs is illustrated in Figure 9.134. In this example, a bipolar transistor with a unit emitter area of 576 μm^2 is compared to a unit-area JFET designed for an I_{DSS} of 20 µA and a pinch-off voltage of 2 V. Each device is biased at 10 µA and operated at $T_A = 25°C$.

The important result is that, under identical quiescent current levels, the change in collector current in bipolar transistors is about 1500 times greater than the change in a JFET's drain current. This explains why FET-input amplifiers behave with less sensitivity to large amplitude HF stimulus. As a result, they offer more RFI rectification immunity.

What all this boils down to is this: Since a user has virtually no access to the amplifier's internal circuitry, the prevention of IC circuit performance degradation due to RFI is left essentially to those means which are external to the ICs.

As the analysis above shows, regardless of the amplifier type, *RFI rectification is directly proportional to the square of the interfering signal's amplitude*. Therefore, to minimize RFI rectification in precision amplifiers, the level of interference must be reduced or eliminated, *prior to the stage*. The most direct way to reduce or eliminate the unwanted noise is by proper filtering.

This topic is covered in the section immediately following.

- **BJT:**

  Emitter area = 576μm²

  I_C = 10μA

  V_T = 25.68mV @ 25°C

$$\Delta i_C = \left(\frac{V_X}{V_T}\right)^2 \bullet \frac{I_C}{4} = \frac{V_X^2}{264}$$

- **JFET:**

  I_{DSS} = 20μA (Z/L=1)

  V_P = 2V

  I_D = 10μA

$$\Delta i_D = \left(\frac{V_X}{V_P}\right)^2 \bullet \frac{I_{DSS}}{2} = \frac{V_X^2}{400x10^3}$$

- **Conclusion: *BJTs ~1500* more *sensitive than JFETs!***

Figure 9.134: *Relative Sensitivity Comparison - BJT Versus JFET*

Reducing RFI Rectification Within Op amp and In-Amp Circuits

EMI and RFI can seriously affect the dc performance of high accuracy analog circuits. Because of their relatively low bandwidth, precision op amps and in-amps simply won't accurately amplify RF signals in the MHz range. However, if these out-of-band signals are allowed to couple into a precision amplifier through either its input, output, or power supply pins, they can be internally rectified by various amplifier junctions, ultimately causing an undesirable dc offset at the output. The previous theoretical discussion of this phenomenon has shown its basic mechanisms. The logical next step is to show how proper filtering can minimize or eliminate these errors.

Elsewhere in this chapter we have discussed how proper supply decoupling minimizes RFI on IC power pins. Further discussion is required with respect to the amplifier inputs and outputs, *at the device level*. It is assumed at this point that system level EMI/RFI approaches have already been implemented, such as an RFI-tight enclosure, properly grounded shields, power rail filtering, etc. The steps following can be considered as circuit-level EMI/RFI prevention.

Op Amp Inputs

The best way to prevent input stage rectification is to use a low-pass filter located close to the op amp input as shown in Figure 9.135. In the case of the inverting op amp at the left, filter capacitor C is placed between equal-value resistors R1-R2. This results in a simple corner frequency expression, as shown in the figure. At very low frequencies or dc, the closed loop gain of the circuit is –R3/(R1+R2). Note that C cannot be connected directly to the inverting input of the op amp, since that would cause instability. The filter bandwidth can be chosen at least 100 times the signal bandwidth to minimize signal loss.

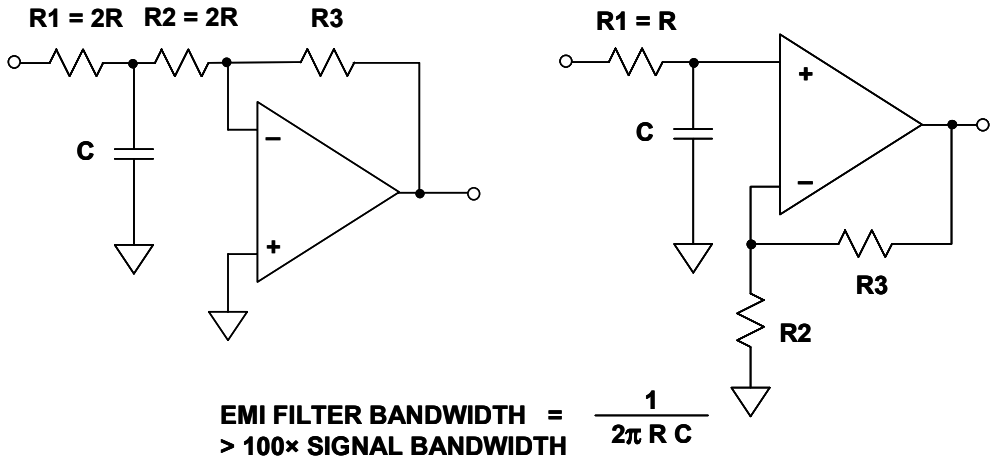


Figure 9.135: *Simple EMI/RFI Noise Filters for Op Amp Circuits*

For the non-inverting case on the right, capacitor C can be connected directly to the op amp input as shown, and an input resistor with a value "R" yields the same corner frequency as the inverting case. In both cases low inductance chip-style capacitors should be used, such as NP0 ceramics. The capacitor should in any case be free of losses or voltage coefficient problems, which limits it to either the NP0 mentioned, or a film type.

It should be noted that a ferrite bead can be used instead of R1, however ferrite bead impedance is not well controlled and is generally no greater than 100 Ω at 10 MHz to 100 MHz. This requires a large value capacitor to attenuate lower frequencies.

In-Amp Inputs

Precision in-amps are particularly sensitive to dc offset errors due to the presence of CM EMI/RFI. This is very much like the problem in op amps. And, as is true with op amps, the sensitivity to EMI/RFI is more acute with the lower power in-amp devices.

A general-purpose approach to proper filtering for device level application of in-amps is shown in Figure 9.136. In this circuit the in-amp could in practice be any one of a number of devices. The relatively complex balanced RC filter preceding the in-amp performs all of the high frequency filtering. The in-amp would be programmed for the gain required in the application, via its gain-set resistance (not shown).

Within the filter, note that fully balanced filtering is provided for both CM (R1-C1 and R2-C2) as well as differential mode (DM) signals (R1+R2, and C3 || the series connection of C1-C2). If R1-R2 and C1-C2 aren't well matched, some of the input common-mode signal at V_{IN} will be converted to a differential mode signal at the in-amp inputs. For this reason, C1 and C2 should be matched to within at least 5% of each other. Also, R1 and R2 should be 1% metal film resistors, so as to aid this matching. It is assumed that the source resistances seen at the V_{IN} terminals are low with respect to R1-R2, and matched. In this type of filter, C3 should be chosen much larger than C1 or C2 (C3 ≥ C1, C2), in order to suppress spurious differential signals due to CM⇒DM conversion resulting from mismatch of the R1-C1 and R2-C2 time constants.

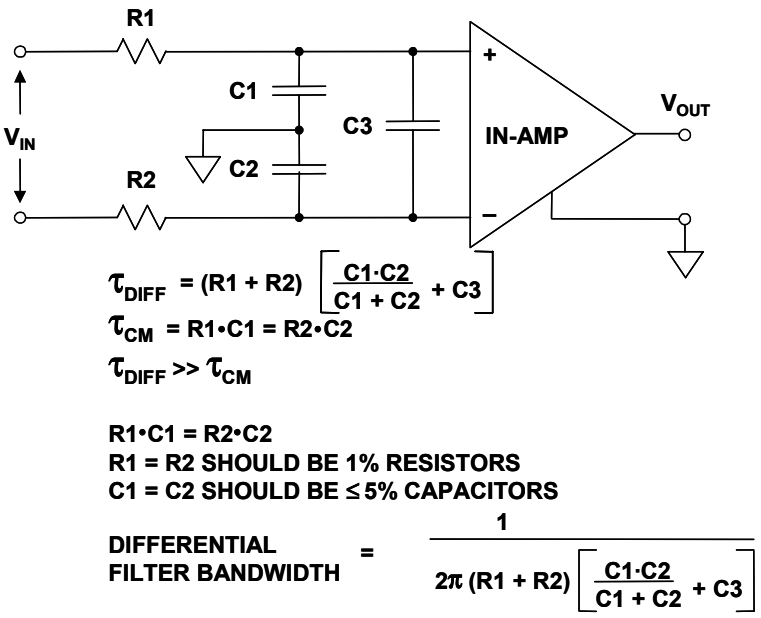
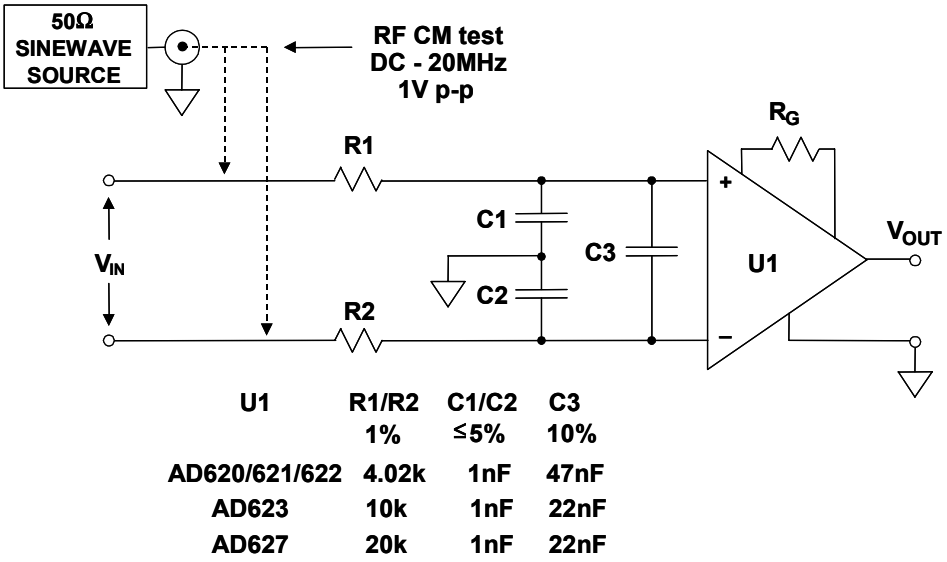


Figure 9.136: *A General-Purpose Common-Mode/Differential-Mode RC EMI/RFI Filter for In-Amps*

The overall filter bandwidth should be at least 100 times the input signal bandwidth. Physically, the filter components should be symmetrically mounted on a PC board with a large area ground plane and placed close to the in-amp inputs for optimum performance.

Figure 9.137 shows a family of these filters, as suited to a range of different in-amps. The RC components should be tailored to the different in-amp devices, as per the table. These filter components are selected for a reasonable balance of low EMI/RFI sensitivity and a low increase in noise (vis-à-vis that of the related in-amp, without the filter).



U1	R1/R2 1%	C1/C2 ≤5%	C3 10%
AD620/621/622	4.02k	1nF	47nF
AD623	10k	1nF	22nF
AD627	20k	1nF	22nF

Figure 9.137: *Flexible Common-Mode and Differential-Mode RC EMI/RFI Filters Are Useful With the AD620 Series, the AD623, AD627, and Other In-Amps*

To test the EMI/RFI sensitivity of the configuration, a 1-Vp-p CM signal can be applied to the input resistors, as noted. With a typically used in-amp such as the AD620 working at a gain of 1000, the maximum RTI input offset voltage shift observed was 1.5 μV over the 20-MHz range. In the AD620 filter example, the differential bandwidth is about 400 Hz.

Common-mode chokes offer a simple, one-component EMI/RFI protection alternative to the passive RC filters, as shown in Figure 9.138.

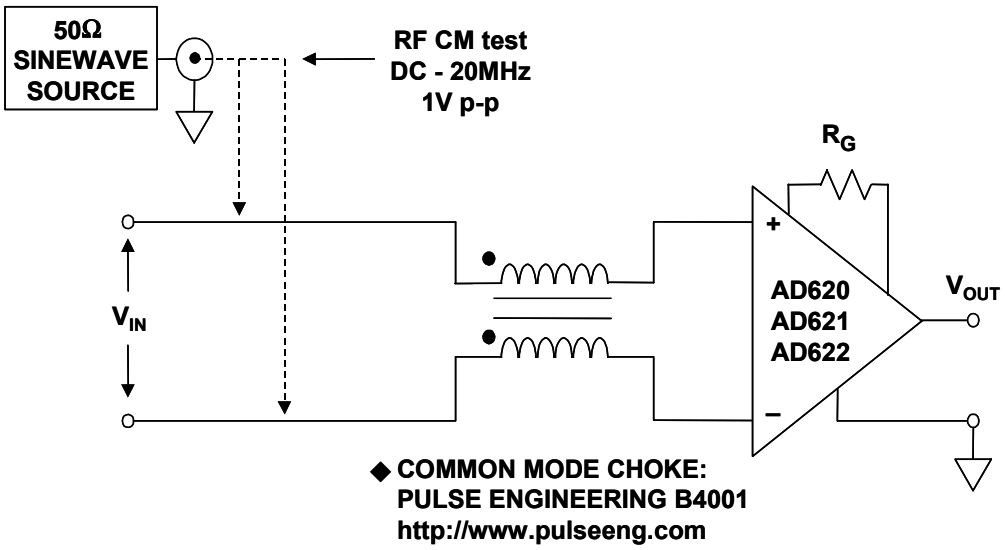


Figure 9.138: *For Simplicity as Well as Lowest Noise EMI/RFI Filter Operation, a Common-Mode Choke is Useful With the AD620 Series In-Amp Devices*

In addition to being a low component count approach, choke-based filters offer low noise, by dispensing with the resistances. Selecting the proper common-mode choke is critical, however. The choke used in the circuit of Figure 9.138 is a Pulse Engineering B4001. The maximum RTI offset shift measured from dc to 20 MHz at G = 1000 was 4.5 μV. Either an off-the-shelf choke such as the B4001 can be used for this filter, or, alternately one can be constructed. Since balance of the windings is important, bifilar wire is suggested. The core material must of course operate over the expected frequency band. Note that, unlike the Figure 9.137 family of RC filters, a choke-only filter offers no differential filtration. Differential mode filtering can be optionally added, with a second stage following the choke, by adding the R1-C3-R2 connections of Figure 9.137.

For further information on in-amp EMI/RFI filtering, see References 10, and 12 - 15.

Amplifier Outputs and EMI/RFI

In addition to filtering the input and power pins, amplifier *outputs* also need to be protected from EMI/RFI, especially if they must drive long lengths of cable, which act as antennas. RF signals received on an output line can couple back into the amplifier input where it is rectified, and appears again on the output as an offset shift.

A resistor and/or ferrite bead, or both, in series with the output is the simplest and least expensive output filter, as shown in Figure 9.139 (upper circuit).

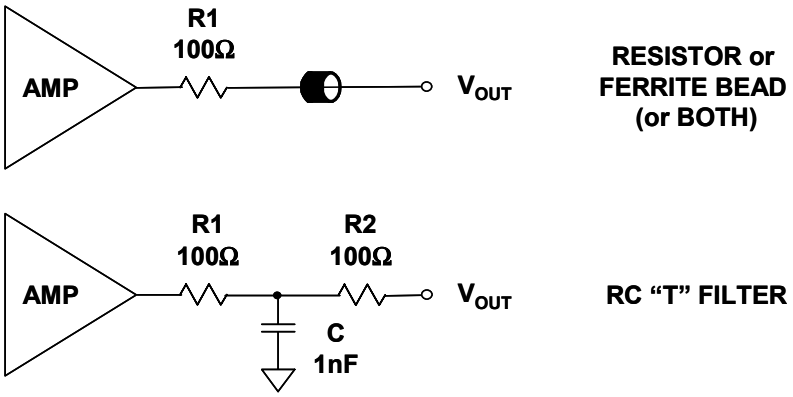


Figure 9.139: *Op Amp and In-Amp Outputs Should be Protected Against EMI/RFI, Particularly if They Drive Long Cables*

Adding a resistor-capacitor-resistor "T" circuit as shown in Figure 9.139 (lower circuit) improves this filter with just slightly more complexity. The output resistor and capacitor divert most of the high frequency energy away from the amplifier, making this configuration useful even with low power active devices. Of course, the time constant of the filter parts must be chosen carefully, to minimize any degradation of the desired output signal. In this case the RC components are chosen for an approximate 3-MHz signal bandwidth, suitable for instrumentation or other low bandwidth stages.

Printed Circuit Board Design for EMI/RFI Protection

This section summarizes general points on EMI/RFI with respect to the printed circuit board (PCB) layout. It complements earlier chapter discussions on general PCB design techniques.

When a PCB design has not been optimized in terms of EMI/RFI, system performance can be compromised. This is true not only for signal-path performance, but also for the system's susceptibility to EMI, plus the degree of EMI radiated by the system. Failure to implement sound PCB layout techniques will very likely lead to system/instrument EMC failures.

To summarize earlier points of this section, a real-world PCB layout may allow multiple paths through which high-frequency noise can couple/radiate into and/or out of the circuit. This is especially true for digital circuitry, operating at high *edge rates*. It is the rapid changes of logic state ($1 \Rightarrow 0$ or $0 \Rightarrow 1$), i.e., the edge rate which contains the HF energy which can easily radiate as EMI. While similar points are applicable to precision high-speed analog or mixed analog/digital circuits, logic devices are by far the worst potential EMI offenders. Identifying critical circuits and paths helps in designing the PCB for both low emissions and susceptibility to radiated and conducted external and internal noise sources.

Choose Logic Devices Carefully!

Logic family speaking, a key point in minimizing system noise problems is to *choose devices no faster than actually required by the application*. Many designers assume that faster is always better—fast logic is better than slow, high bandwidth amplifiers better than low bandwidth ones, and fast DACs and ADCs are better, even if the speed isn't required by the system. Unfortunately, faster is *not* better, and actually may be worse for EMI concerns.

Many fast DACs and ADCs have digital inputs and outputs with edge rates in the 1-V/ns region. Because of this wide bandwidth, the sampling clock and the digital inputs can respond to any form of high frequency noise, even glitches as narrow as 1 to 3 ns. These high speed data converters and amplifiers are thus easy prey for the high frequency noise of microprocessors, digital signal processors, motors, switching regulators, hand-held radios, electric jackhammers, etc. With some of these high-speed devices, a small amount of input/output filtering may be required to desensitize the circuit from its EMI/RFI environment. A ferrite bead just before the local decoupling capacitor is very effective in filtering high frequency noise on supply lines. Of course, with circuits requiring bipolar supplies, this technique should be applied to both positive and negative supply lines.

To help reduce emissions generated by extremely fast moving digital signals at DAC inputs or ADC outputs, a small resistor or ferrite bead may be required at each digital input/output.

Design PCBs Thoughtfully

Once the system's critical paths and circuits have been identified, the next step in implementing sound PCB layout is to partition the printed circuit board according to circuit function. This involves the appropriate use of power, ground, and signal planes. Good PCB layouts also isolate critical analog paths from sources of high interference (I/O lines and connectors, for example). High frequency circuits (analog and digital) should be separated from low frequency ones. Furthermore, automatic signal routing CAD layout software should be used with extreme caution. Critical signal paths should be routed by hand, to avoid undesired coupling and/or emissions.

Properly designed multilayer PCBs can reduce EMI emissions and increase immunity to RF fields, by a factor of 10 or more, compared to double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted with signal crossovers, etc. If the system has separate analog and digital ground and power planes, the analog ground plane should be underneath the analog power plane, and similarly, the digital ground plane should be underneath the digital power plane. There should be no overlap between analog and digital ground planes, nor analog and digital power planes.

Designing Controlled Impedances Traces on PCBs

A variety of trace geometries are possible with controlled impedance designs, and they may be either integral to or allied to the PCB pattern. In the discussions below, the basic patterns follow those of the IPC, as described in standard 2141 (see Reference 16).

Note that the figures below use the term "ground plane". It should be understood that this plane is in fact a large area, low impedance *reference* plane. In practice it may actually be either a ground plane or a power plane, both of which are assumed to be at zero ac potential.

The first of these is the simple wire-over-a-plane form of transmission line, also called a *wire microstrip*. A cross-sectional view is shown in Figure 9.140. This type of transmission line might be a signal wire used within a breadboard, for example. It is composed simply of a discrete insulated wire spaced a fixed distance over a ground plane. The dielectric would be either the insulation wall of the wire, or a combination of this insulation and air.

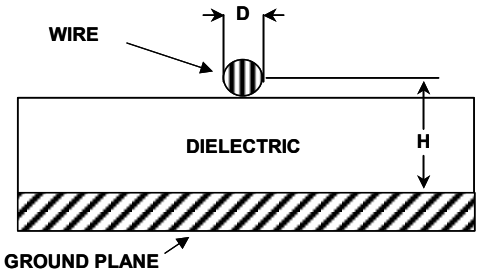


Figure 9.140: *A Wire Microstrip Transmission Line With Defined Impedance is Formed by an Insulated Wire Spaced From a Ground Plane*

The impedance of this line in ohms can be estimated with Eq. 9.20. Here D is the conductor diameter, H the wire spacing above the plane, and ε_r the dielectric constant.

$$Z_o(\Omega) = \frac{60}{\sqrt{\varepsilon_r}} \ln\left[\frac{4H}{D}\right] . \qquad \text{Eq. 9.20}$$

For patterns integral to the PCB, there are a variety of geometric models from which to choose, single-ended and differential. These are covered in some detail within IPC standard 2141 (see Reference 16), but information on two popular examples is shown here.

Before beginning any PCB-based transmission line design, it should be understood that there are abundant equations, all claiming to cover such designs. In this context, "Which of these are accurate?" is an extremely pertinent question. The unfortunate answer is, *none are perfectly so!* All of the existing equations are approximations, and thus accurate to varying degrees, depending upon specifics. The best known and most widely quoted equations are those of Reference 16, but even these come with application caveats.

Reference 17 has evaluated the Reference 16 equations for various geometric patterns against test PCB samples, finding that predicted accuracy varies according to target impedance. Reference 18 also evaluates the Reference 16 equations, offering an alternative and even more complex set (see Reference 19). The equations quoted below are from Reference 16, and are offered here as a starting point for a design, subject to

further analysis, testing and design verification. The bottom line is, study carefully, and take PCB trace impedance equations with a proper dose of salt.

Microstrip PCB Transmission Lines

For a simple two-sided PCB design where one side is a ground plane, a signal trace on the other side can be designed for controlled impedance. This geometry is known as a *surface microstrip,* or more simply, *microstrip*.

A cross-sectional view of a two-layer PCB illustrates this microstrip geometry as shown in Figure 9.141.

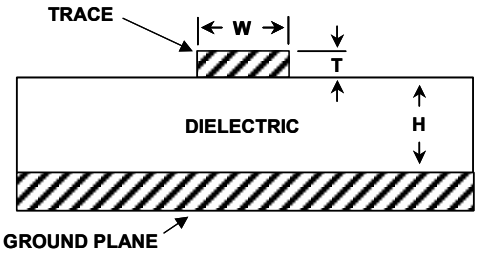


Figure 9.141: *A Microstrip Transmission Line With Defined Impedance is Formed by a PCB Trace of Appropriate Geometry, Spaced From a Ground Plane*

For a given PCB laminate and copper weight, note that all parameters will be predetermined except for W, the width of the signal trace. Eq. 9.21 can then be used to design a PCB trace to match the impedance required by the circuit. For the signal trace of width W and thickness T, separated by distance H from a ground (or power) plane by a PCB dielectric with dielectric constant ε_r, the characteristic impedance is:

$$Z_o(\Omega) = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left[\frac{5.98H}{(0.8W + T)}\right] \qquad \text{Eq. 9.21}$$

Note that in these expressions, measurements are in common dimensions (mils).

These transmission lines will have not only a characteristic impedance, but also capacitance. This can be calculated in terms of pF/in as shown in Eq. 9.22.

$$C_o(\text{pF/in}) = \frac{0.67(\varepsilon_r + 1.41)}{\ln[5.98H/(0.8W + T)]} \qquad \text{Eq. 9.22}$$

As an example including these calculations, a 2-layer board might use 20-mil wide (W), 1 ounce (T=1.4) copper traces separated by 10-mil (H) FR-4 ($\varepsilon_r = 4.0$) dielectric material. The resulting impedance for this microstrip would be about 50 Ω. For other standard impedances, for example the 75-Ω video standard, adjust "W" to about 8.3 mils.

Some Microstrip Guidelines

This example touches an interesting and quite handy point. Reference 17 discusses a useful guideline pertaining to microstrip PCB impedance. For a case of dielectric constant of 4.0 (FR-4), it turns out that when W/H is 2/1, the resulting impedance will be close to 50 Ω (as in the first example, with W=20 mils).

Careful readers will note that Eq. 9.21 predicts Z_o to be about 46 Ω, generally consistent with accuracy quoted in Reference 17 (>5%). The IPC microstrip equation is most accurate between 50 and 100 Ω, but is substantially less so for lower (or higher) impedances. Reference 20 gives tabular results of various PCB industry impedance calculator tools.

The propagation delay of the microstrip line can also be calculated, as per Eq. 9.23. This is the one-way transit time for a microstrip signal trace. Interestingly, for a given geometry model, *the delay constant in ns/ft is a function only of the dielectric constant, and not the trace dimensions* (see Reference 21). Note that this is quite a convenient situation. It means that, with a given PCB laminate (and given ε_r), the propagation delay constant is fixed for various impedance lines.

$$t_{pd}(\text{ns/ft}) = 1.017\sqrt{0.475\varepsilon_r + 0.67} \qquad \text{Eq. 9.23}$$

This delay constant can also be expressed in terms of ps/in, a form which will be more practical for smaller PCBs. This is:

$$t_{pd}(\text{ps/in}) = 85\sqrt{0.475\varepsilon_r + 0.67} \qquad \text{Eq. 9.24}$$

Thus for an example PCB dielectric constant of 4.0, it can be noted that a microstrip's delay constant is about 1.63 ns/ft, or 136 ps/in. These two additional rules-of-thumb can be useful in designing the timing of signals across PCB trace runs.

Symmetric Stripline PCB Transmission Lines

A method of PCB design preferred from many viewpoints is a multi-layer PCB. This arrangement *embeds* the signal trace between a power and a ground plane, as shown in the cross-sectional view of Figure 9.142. The low-impedance ac-ground planes and the embedded signal trace form a *symmetric stripline* transmission line.

As can be noted from the figure, the return current path for a high frequency signal trace is located directly above and below the signal trace on the ground/power planes. The high frequency signal is thus contained entirely inside the PCB, minimizing emissions, and providing natural shielding against incoming spurious signals.

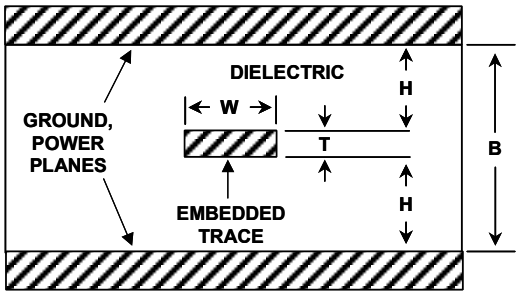


Figure 9.142: *A Symmetric Stripline Transmission Line With Defined Impedance is Formed by a PCB Trace of Appropriate Geometry Embedded Between Equally Spaced Ground and/or Power Planes*

The characteristic impedance of this arrangement is again dependent upon geometry and the ε_r of the PCB dielectric. An expression for Z_O of the stripline transmission line is:

$$Z_o(\Omega) = \frac{60}{\sqrt{\varepsilon_r}} \ln\left[\frac{1.9(B)}{(0.8W + T)}\right]. \qquad \text{Eq. 9.25}$$

Here, all dimensions are again in mils, and B is the spacing between the two planes. In this symmetric geometry, note that B is also equal to 2H + T. Reference 17 indicates that the accuracy of this Reference 16 equation is typically on the order of 6%.

Another handy guideline for the symmetric stripline in an $\varepsilon_r = 4.0$ case is to make B a multiple of W, in the range of 2 to 2.2. This will result in an stripline impedance of about 50Ω. Of course this rule is based on a further approximation, by neglecting T. Nevertheless, it is still useful for ballpark estimates.

The symmetric stripline also has a characteristic capacitance, which can be calculated in terms of pF/in as shown in Eq. 9.26.

$$C_o(\text{pF/in}) = \frac{1.41(\varepsilon_r)}{\ln[3.81H/(0.8W + T)]} \quad . \qquad \text{Eq. 9.26}$$

The propagation delay of the symmetric stripline is shown in Eq. 9.27.

$$t_{pd}(\text{ns/ft}) = 1.017\sqrt{\varepsilon_r} \qquad \text{Eq. 9.27}$$

or, in terms of ps:

$$t_{pd}(\text{ps/in}) = 85\sqrt{\varepsilon_r} \qquad \text{Eq. 9.28}$$

For a PCB dielectric constant of 4.0, it can be noted that the symmetric stripline's delay constant is almost exactly 2 ns/ft, or 170 ps/in.

Some Pros and Cons of Embedding Traces

The above discussions allow the design of PCB traces of defined impedance, either on a surface layer or embedded between layers. There of course are many other considerations beyond these impedance issues.

Embedded signals do have one major and obvious disadvantage— the debugging of the hidden circuit traces is difficult to impossible. Some of the pros and cons of embedded signal traces are summarized in Figure 9.143.

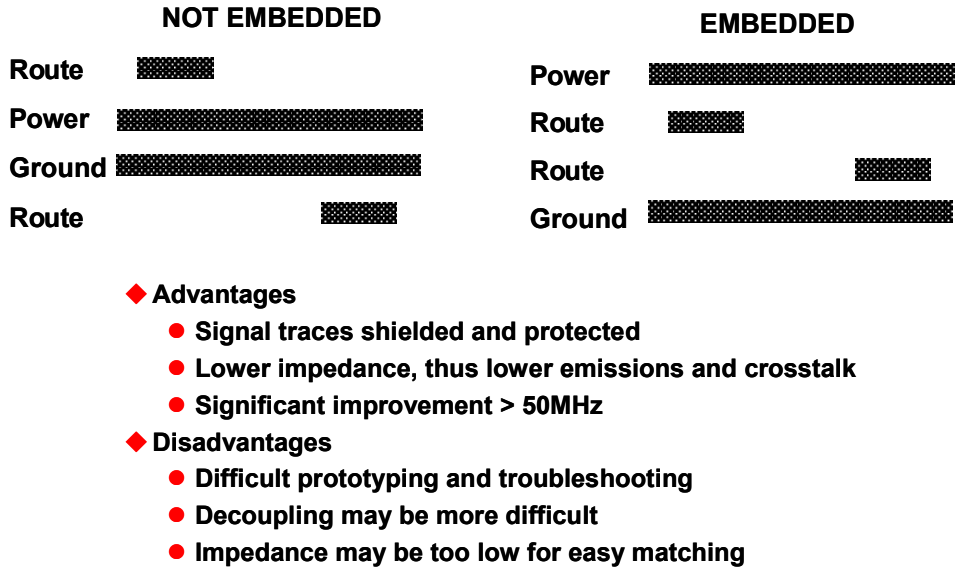


Figure 9.143: *The Pros and Cons of Not Embedding Vs. the Embedding of Signal Traces in Multi-Layer PCB Designs*

Multi-layer PCBs can be designed *without* the use of embedded traces, as is shown in the left-most cross-sectional example. This embedded case could be considered as a doubled two-layer PCB design (i.e., four copper layers overall). The routed traces at the top form a microstrip with the power plane, while the traces at the bottom form a microstrip with the ground plane. In this example, the signal traces of both outer layers are readily accessible for measurement and troubleshooting purposes. But, the arrangement does nothing to take advantage of the shielding properties of the planes.

This non embedded arrangement will have greater emissions and susceptibility to external signals, vis-a-vis the embedded case at the right, which uses the embedding, and does take full advantage of the planes. As in many other engineering efforts, the decision of embedded vs. not-embedded for the PCB design becomes a tradeoff, in this case one of reduced emissions vs. ease of testing.

Dealing with High-Speed Logic

Much has been written about terminating PCB traces in their characteristic impedance, to avoid signal reflections. A good guideline to determine when this is necessary is as follows: *Terminate the transmission line in its characteristic impedance when the one-way propagation delay of the PCB track is equal to or greater than one-half the applied*

signal rise/fall time (whichever edge is faster). For example, a 2 inch microstrip line over an $E_r = 4.0$ dielectric would have a delay of ~270 ps. Using the above rule strictly, termination would be appropriate whenever the signal rise time is < ~500 ps. A more conservative rule is to use a 2 inch (PCB track length)/nanosecond (rise/fall time) rule. If the signal trace exceeds this trace-length/speed criterion, then termination should be used.

For example, PCB tracks for high-speed logic with rise/fall time of 5 ns should be terminated in their characteristic impedance if the track length is equal to or greater than 10 inches (where measured length *includes* meanders).

As an example of what can be expected today in modern systems, Figure 9.143 shows typical rise/fall times for several logic families including the SHARC DSPs operating on +3.3V supplies. As would be expected, the rise/fall times are a function of load capacitance.

- **GaAs: 0.1ns**
- **ECL: 0.75ns**
- **ADI SHARC DSPs: 0.5 ns to 1 ns (Operating on +3.3V Supply)**

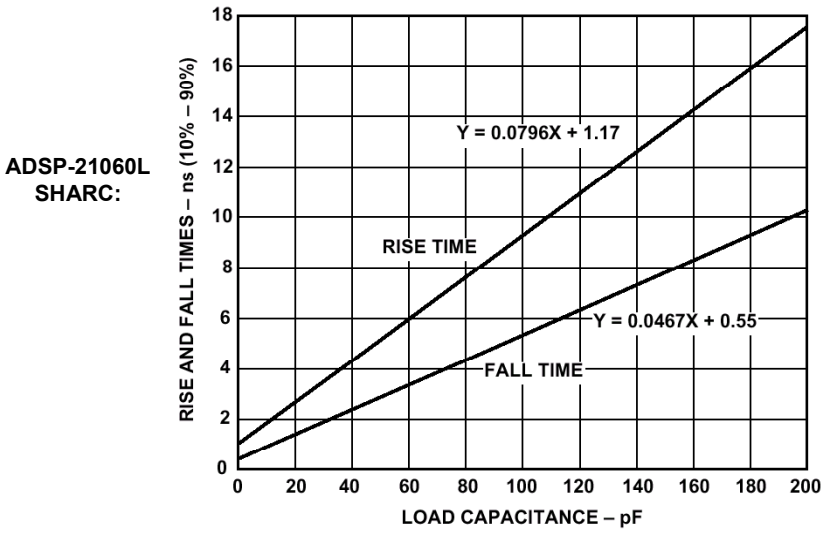


Figure 9.143: *Typical DSP Output Rise Times and Fall Times*

In the analog domain, it is important to note that this same 2 inch/nanosecond guideline should also be used with op amps and other circuits, to determine the need for transmission line techniques. For instance, if an amplifier must output a maximum frequency of f_{max}, then the equivalent risetime t_r is related to this f_{max}. This limiting risetime, t_r, can be calculated as:

$$t_r = 0.35/f_{max} \qquad \text{Eq. 9.29}$$

The maximum PCB track length is then calculated by multiplying t_r by 2 inch/nanosecond. For example, a maximum frequency of 100 MHz corresponds to a risetime of 3.5 ns, so a 7-inch or more track carrying this signal should be treated as a transmission line.

The best ways to keep sensitive analog circuits from being affected by fast logic are to physically separate the two by the PCB layout, and to use no faster logic family than is dictated by system requirements. In some cases, this may require the use of several logic families in a system. An alternative is to use series resistance or ferrite beads to slow down the logic transitions where highest speed isn't required. Figure 9.145 shows two methods.

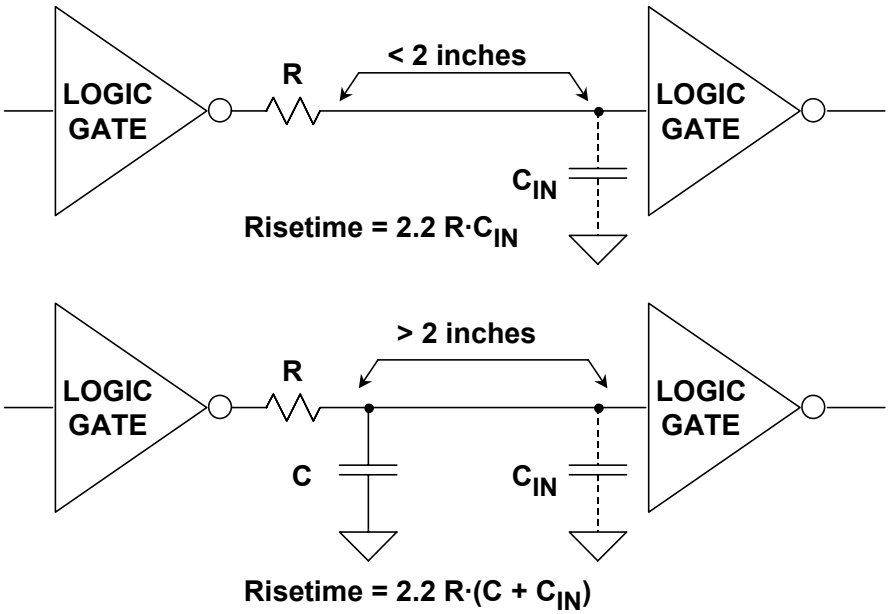


Figure 9.145: *Damping Resistors Slow Down Fast Logic Edges to Minimize EMI/RFI Problems*

In the first, the series resistance and the input capacitance of the gate form a lowpass filter. Typical CMOS input capacitance is 5 pF to10 pF. Locate the series resistor close to the driving gate. The resistor minimizes transient currents and may eliminate the necessity of using transmission line techniques. The value of the resistor should be chosen such that the rise and fall times at the receiving gate are fast enough to meet system requirement, but no faster. Also, make sure that the resistor is not so large that the logic levels at the receiver are out of specification because of the voltage drop caused by the source and sink current which flow through the resistor. The second method is suitable for longer distances (>2 inches), where additional capacitance is added to slow down the edge speed. Notice that either one of these techniques increases delay and increases the rise/fall time of the original signal. This must be considered with respect to the overall timing budget, and the additional delay may not be acceptable.

Figure 9.146 shows a situation where several DSPs must connect to a single point, as would be the case when using read or write strobes bidirectionally connected from several DSPs. Small damping resistors shown in Figure 9.146A can minimize ringing provided the length of separation is less than about 2 inches. This method will also increase rise/fall times and propagation delay. If two groups of processors must be connected, a single resistor between the pairs of processors as shown in Figure 9.146B can serve to damp out ringing.

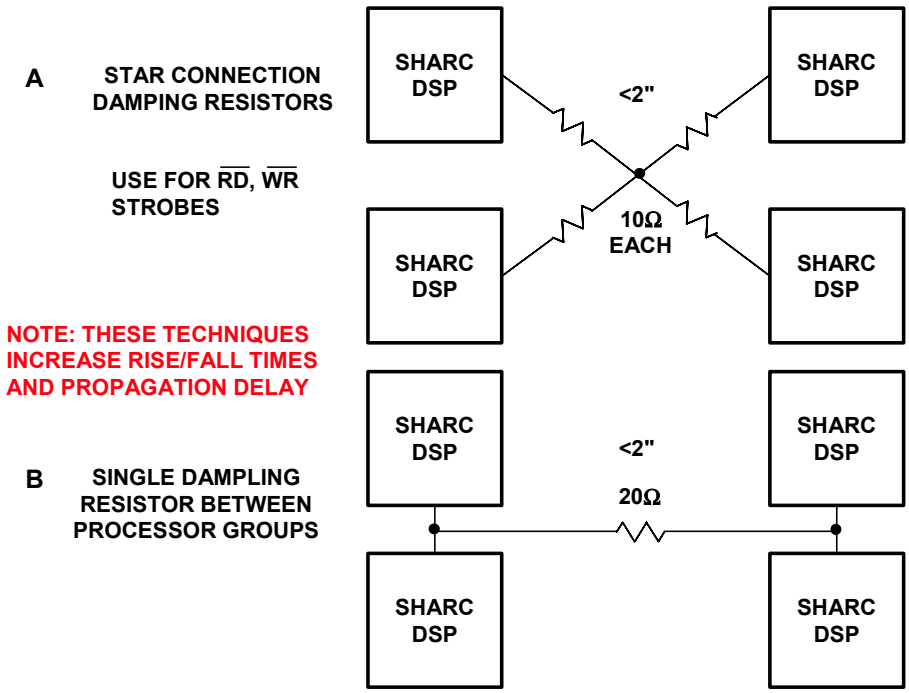


Figure 9.146: *Series Damping Resistors for High Speed DSP Interconnections*

The only way to preserve 1-ns or less rise/fall times over distances greater than about 2 inches without ringing is to use transmission line techniques. Figure 9.147 shows two popular methods of termination: end termination, and source termination. The end termination method (Figure 9.147A) terminates the cable at its terminating point in the characteristic impedance of the microstrip transmission line. Although higher impedances can be used, 50 Ω is popular because it minimizes the effects of the termination impedance mismatch due to the input capacitance of the terminating gate (usually 5 pF to 10 pF).

In Figure 9.147A, the cable is terminated in a Thevenin impedance of 50 Ω terminated to +1.4 V (the midpoint of the input logic threshold of 0.8 V and 2.0 V). This requires two resistors (91 Ω and 120 Ω), which add about 50 mW to the total quiescent power dissipation to the circuit. Figure 9.147A also shows the resistor values for terminating with a +5V supply (68 Ω and 180 Ω). Note that 3.3-V logic is much more desirable in line driver applications because of its symmetrical voltage swing, faster speed, and lower power. Drivers are available with less than 0.5-ns time skew, source and sink current capability greater than 25 mA, and rise/fall times of about 1 ns. Switching noise generated by 3.3-V logic is generally less than 5-V logic because of the reduced signal swings and lower transient currents.

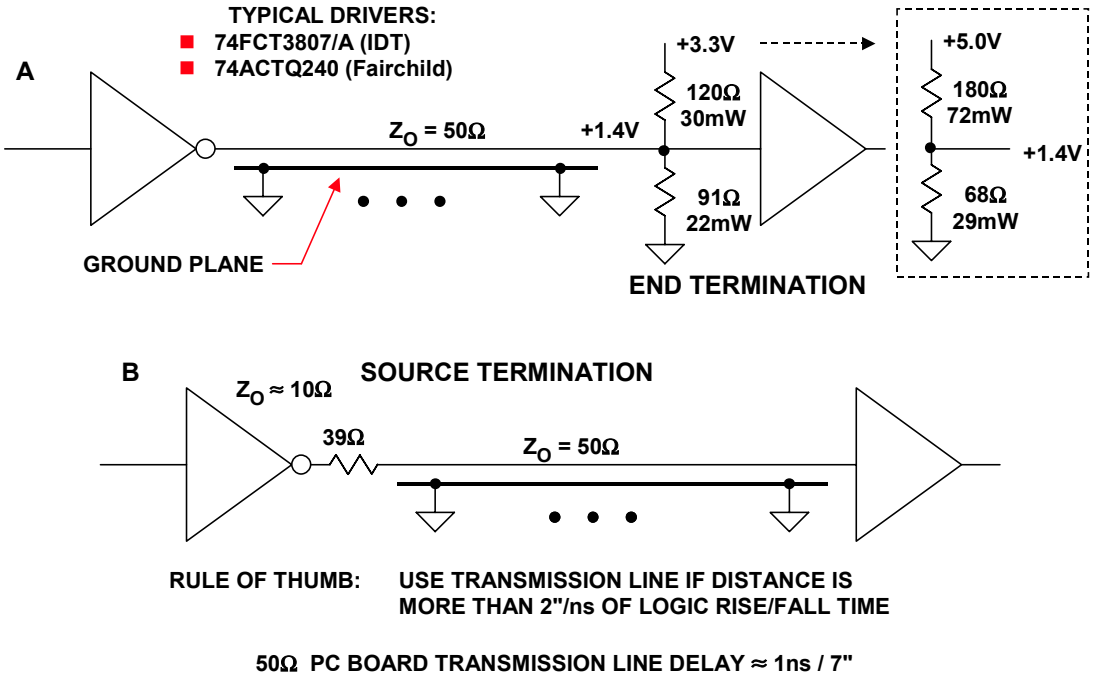


Figure 9.147: *Termination Techniques for Controlled Impedance Microstrip Transmission Lines*

The source termination method, shown in Figure 9.147B, absorbs the reflected waveform with an impedance equal to that of the transmission line. This requires about 39 Ω in series with the internal output impedance of the driver, which is generally about 10 Ω. This technique requires that the end of the transmission line be terminated in an open circuit, therefore no additional fanout is allowed. The source termination method adds no additional quiescent power dissipation to the circuit.

Figure 9.148 shows a method for distributing a high speed clock to several devices. The problem with this approach is that there is a small amount of time skew between the clocks because of the propagation delay of the microstrip line (approximately 1 ns /7"). This time skew may be critical in some applications. It is important to keep the stub length to each device less than 0.5" in order to prevent mismatches along the transmission line.

The clock distribution method shown in Figure 9.149 minimizes the clock skew to the receiving devices by using source terminations and making certain the length of each microstrip line is equal. There is no extra quiescent power dissipation as would be the case using end termination resistors.

Figure 9.150 shows how source terminations can be used in bi-directional link port transmissions between SHARC DSPs. The output impedance of the SHARC driver is approximately 17 Ω, and therefore a 33-Ω series resistor is required on each end of the transmission line for proper source termination.

The method shown in Figure 9.151 can be used for bi-directional transmission of signals from several sources over a relatively long transmission line. In this case, the line is terminated at both ends, resulting in a dc load impedance of 25 Ω. SHARC drivers are capable of driving this load to valid logic levels.

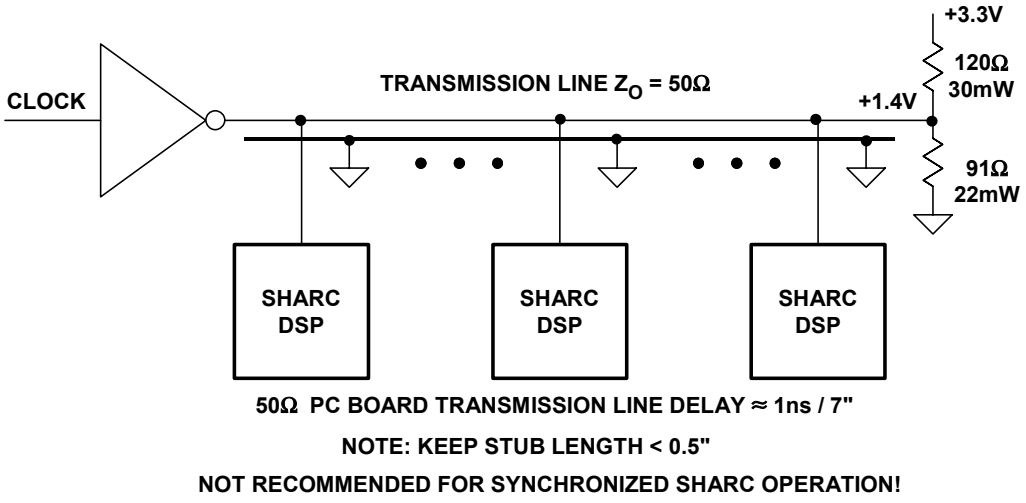


Figure 9.148: *Clock Distribution Using End-of-Line Termination*

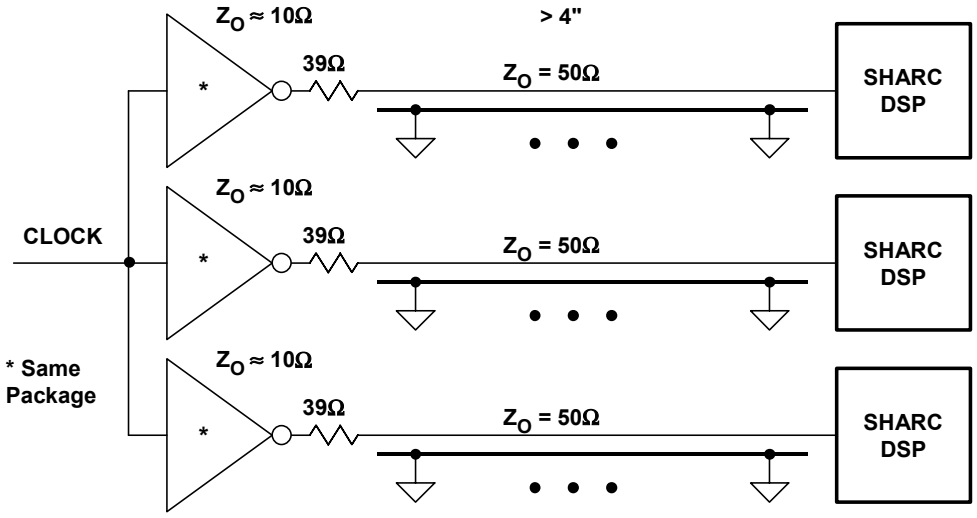


Figure 9.149: *Preferred Method of Clock Distribution Using Source Terminated Transmission Lines*

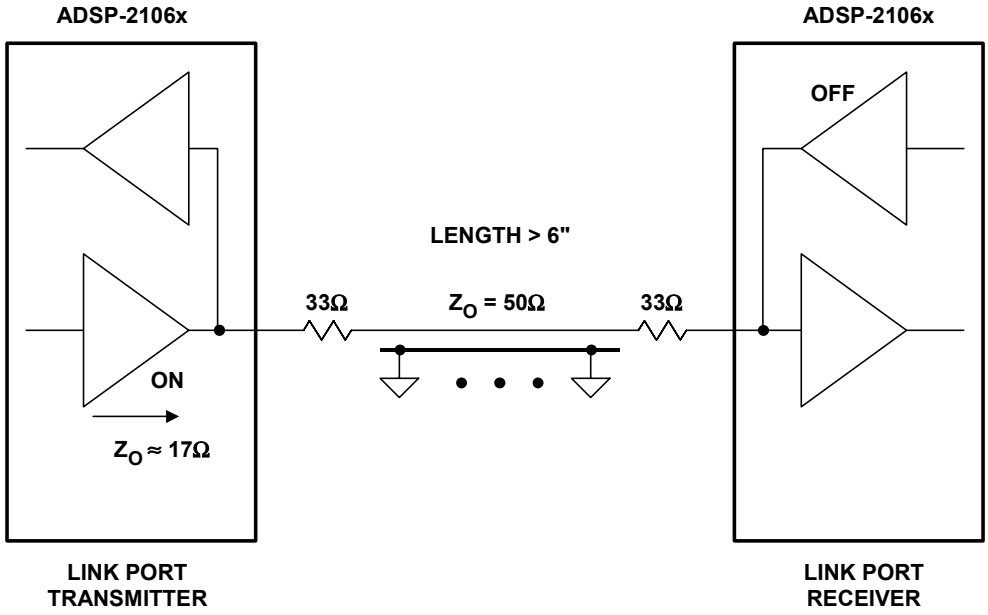


Figure 9.150: *Source Termination for Bi-Directional Transmission Between SHARC DSPs*

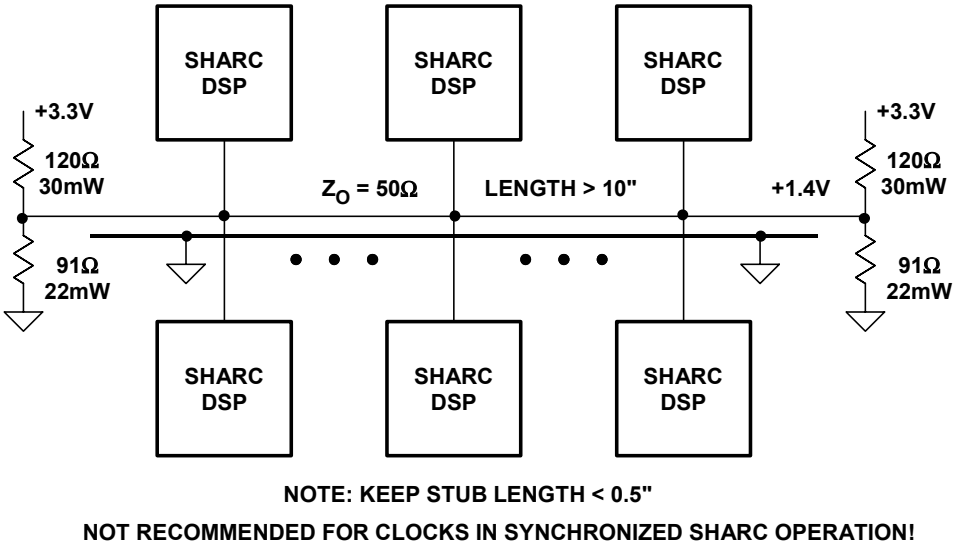


Figure 9.151: *Single Transmission Line Terminated at Both Ends*

Emitter-coupled-logic (ECL) has long been known for low noise and its ability to drive terminated transmission lines with rise/fall times less than 2 ns. The family presents a constant load to the power supply, and the low-level differential outputs provide a high degree of common-mode rejection. However, ECL dissipates lots of power.

Recently, low-voltage-differential-signaling (LVDS) logic has attained widespread popularity because of similar characteristics, but with lower amplitudes and lower power dissipation than ECL. The defining LVDS specification can be found in Reference 23, and References 24 and 25 should also prove useful. The LVDS logic swing is typically 350 mV peak-to-peak centered about a common-mode voltage of +1.2 V. A typical driver

and receiver configuration is shown in Figure 9.152. The driver consists of a nominal 3.5-mA current source with polarity switching provided by PMOS and NMOS transistors as in the case of the AD9430 12-bit, 170-/210-MSPS ADC. The output voltage of the driver is nominally 350 mV peak-to-peak at each output, and can vary between 247 mV and 454 mV. The output current can vary between 2.47 mA and 4.54 mA. The LVDS receiver is terminated in a 100 Ω line-to-line. According to the LVDS specification, the receiver must respond to signals as small as 100 mV, over a common-mode voltage range of 50 mV to +2.35 V. The wide common-mode receiver voltage range is to accommodate ground voltage differences up to ±1 V between the driver and receiver.

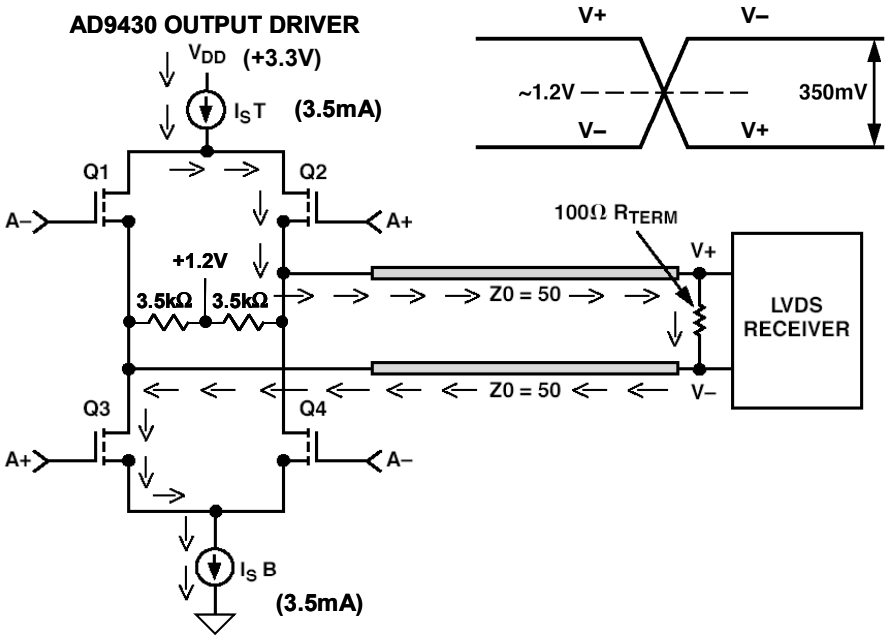


Figure 9.152: *LVDS Driver and Receiver*

The LVDS edge speed is defined as the 20% to 90% rise/fall time (as opposed to 10% to 90% for CMOS logic) and specified to be less than < 0.3 t_{ui}, where t_{ui} is the inverse of the data signaling rate. For a 210 MSPS sampling rate, t_{ui} = 4.76 ns, and the 20% to 80% rise/fall time must be less than 0.3 × 4.76 = 1.43 ns. For the AD9430, the rise/fall time is nominally 0.5 ns.

LVDS outputs for high-performance ADCs should be treated differently than standard LVDS outputs used in digital logic. While standard LVDS can drive 1 to 10 meters in high-speed digital applications (dependent on data rate), it is not recommended to let a high-performance ADC drive that distance. It is recommended to keep the output trace lengths short (< 2 in.), minimizing the opportunity for any noise coupling onto the outputs from the adjacent circuitry, which may get back to the analog inputs. The differential output traces should be routed close together, maximizing common-mode rejection, with the 100 Ω termination resistor close to the receiver. Users should pay attention to PCB trace lengths to minimize any delay skew. A typical differential microstrip PCB trace cross section is shown in Figure 9.153 along with some recommended layout guidelines.

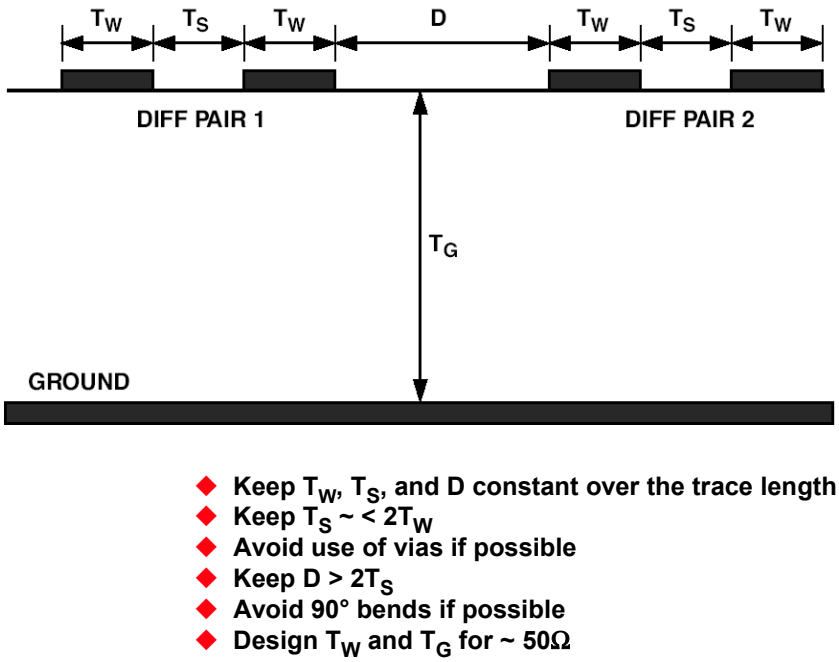


Figure 9.153: *Microstrip PCB Layout for Two Pairs of LVDS Signals*

LVDS also offers some benefits in reduced EMI. The EMI fields generated by the opposing LVDS currents tend to cancel each other (for matched edge rates). In high speed ADCs, LVDS offers simpler timing constraints compared to demultiplexed CMOS outputs at similar data rates. A demultiplexed data bus requires a synchronization signal that is not required in LVDS. In demuxed CMOS buses, a clock equal to one-half the ADC sample rate is needed, adding cost and complexity, that is not required in LVDS.

REFERENCES:
9.6 EMI/RFI CONSIDERATIONS

1. Tim Williams, **EMC for Product Designers, 2nd Ed.**, Newnes, Oxford, 1996, ISBN: 0 7506 2466 3.

2. Henry Ott, **Noise Reduction Techniques In Electronic Systems**, **2nd Ed.**, John Wiley & Sons, New York, 1988, ISBN 0-471-85068-3.

3. Mark Montrose, **EMC and the Printed Circuit Board**, IEEE Press, 1999, ISBN 0-7803-4703-X.

4. Ralph Morrison, **Grounding And Shielding Techniques in Instrumentation, 3rd Ed.**, John Wiley & Sons, New York, 1986, ISBN 0-471-83805-5.

5. Daryl Gerke and William Kimmel, "Designer's Guide to Electromagnetic Compatibility," **EDN**, January 20, 1994.

6. **Designing for EMC** (Workshop Notes), Kimmel Gerke Associates, Ltd., 1994.

7. Daryl Gerke and William Kimmel, "EMI and Circuit Components," **EDN**, September 1, 2000.

8. Alan Rich, "Understanding Interference-Type Noise," **Analog Dialogue**, Vol. 16, No. 3, 1982, pp. 16-19 (also available as application note AN346).

9. Alan Rich, "Shielding and Guarding," **Analog Dialogue**, Vol. 17, No. 1, 1983, pp. 8-13 (also available as application note AN347).

10. James Wong, Joe Buxton, Adolfo Garcia, James Bryant**,** "Filtering and Protection Against EMI/RFI" and "Input Stage RFI Rectification Sensitivity", Chapter 1, pg. 21-55 of **Systems Application Guide**, 1993, Analog Devices, Inc., Norwood, MA, ISBN 0-916550-13-3.

11. Adolfo Garcia**,** "EMI/RFI Considerations"**,** Chapter 7, pg 69-88 of **High Speed Design Techniques**, 1996, Analog Devices, Inc., Norwood, MA, 1993, ISBN 0-916550-17-6.

12. Walt Kester, Walt Jung, Chuck Kitchen, "Preventing RFI Rectification"**,** Chapter 10, pg 10.39-10.43 of **Practical Design Techniques for Sensor Signal Conditioning**, Analog Devices, Inc., Norwood, MA, 1999, ISBN 0-916550-20-6.

13. Charles Kitchen, Lew Counts, **A Designer's Guide to Instrumentation Amplifiers**, Analog Devices, Inc., 2000.

14. **B4001 and B4003 common-mode chokes**, Pulse Engineering, Inc., 12220 World Trade Drive, San Diego, CA, 92128, 619-674-8100, http://www.pulseeng.com

15. **Understanding Common Mode Noise**, Pulse Engineering, Inc., 12220 World Trade Drive, San Diego, CA, 92128, 619-674-8100, http://www.pulseeng.com

16. Standard IPC-2141, "Controlled Impedance Circuit Boards and High Speed Logic Design," 1996, Institute for Interconnection and Packaging Electronic Circuits, 2215 Sanders Road, Northbrook, IL, 60062-6135, (847) 509-9700, http://www.ipc.org

17. Eric Bogatin, "Verifying the Accuracy of 2D Field Solvers for Characteristic Impedance Calculation," Ansoft Seminar, October 11, 2000, http://www.bogatinenterprises.com

18. Andrew Burkhardt, Christopher Gregg, Alan Staniforth, "Calculation of PCB Track Impedance," Technical Paper S-19-5, presented at the IPC Printed Circuits Expo '99 Conference, March 14–18, 1999

19. Brian C. Wadell, **Transmission Line Design Handbook,** Artech House, Norwood, MA, 1991, ISBN: 0-89006-436-9

20. Eric Bogatin, "No Myths Allowed, "Impedance Calculations"," a Chip Center column", November 1, 1999, http://www.chipcenter.com/signalintegrity

21. William R. Blood, Jr., **MECL System Design Handbook** (HB205/D, Rev. 1A May 1988), ON Semiconductor, August, 2000.

22. Paul Brokaw, "An IC Amplifier User Guide To Decoupling, Grounding, And Making Things Go Right For A Change," **Analog Devices AN202**.

23. TIA/EIA-644-A Standard, **Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits**, January 30, 2001.

24. IEEE Std. 1596.3-1996, **IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface**, IEEE, 1996.

25. Cindy Bloomingdale and Gary Hendrickson, "LVDS Data Outputs for High-Speed Analog-to-Digital Converter," **Application Note AN-586**, Analog Devices, 2002.

Some useful EMC and signal integrity related URLs:

Eric Bogatin website, http://www.bogatinenterprises.com

Chip Center's "Signal Integrity" page, http://www.chipcenter.com/signalintegrity

Kimmel Gerke Associates website, http://www.emiguru.com

Henry Ott website, http://www.hottconsultants.com

IEEE EMC website, http://www.ewh.ieee.org/soc/emcs

Mark Montrose website, http://www.montrosecompliance.com/index.html

Tim Williams website, http://www.elmac.co.uk

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NOTES:

SECTION 9.7: LOW VOLTAGE LOGIC INTERFACING

Walt Kester, Ethan Bordeax, Johannes Horvath, Catherine Redmond, Eva Murphy

For nearly 20 years, the standard V_{DD} for digital circuits was 5 V. This voltage level was used because bipolar transistor technology required 5 V to allow headroom for proper operation. However, in the late 1980s, Complimentary Metal Oxide Semiconductor (CMOS) became the standard for digital IC design. This process did not necessarily require the same voltage levels as TTL circuits, but the industry adopted the 5-V TTL standard logic threshold levels to maintain backward compatibility with older systems (Reference 1).

The current revolution in supply voltage reduction has been driven by demand for faster and smaller products at lower costs. This push has caused silicon geometries to drop from 2 μm in the early 1980s to 0.18 μm that is used in today's latest microprocessor and IC designs. As feature sizes have become increasingly smaller, the voltage for optimum device performance has also dropped below the 5-V level. This is illustrated in the current microprocessors for PCs, where the optimum core operating voltage is programmed externally using voltage identification (VID) pins, and can be as low as 1.3 V.

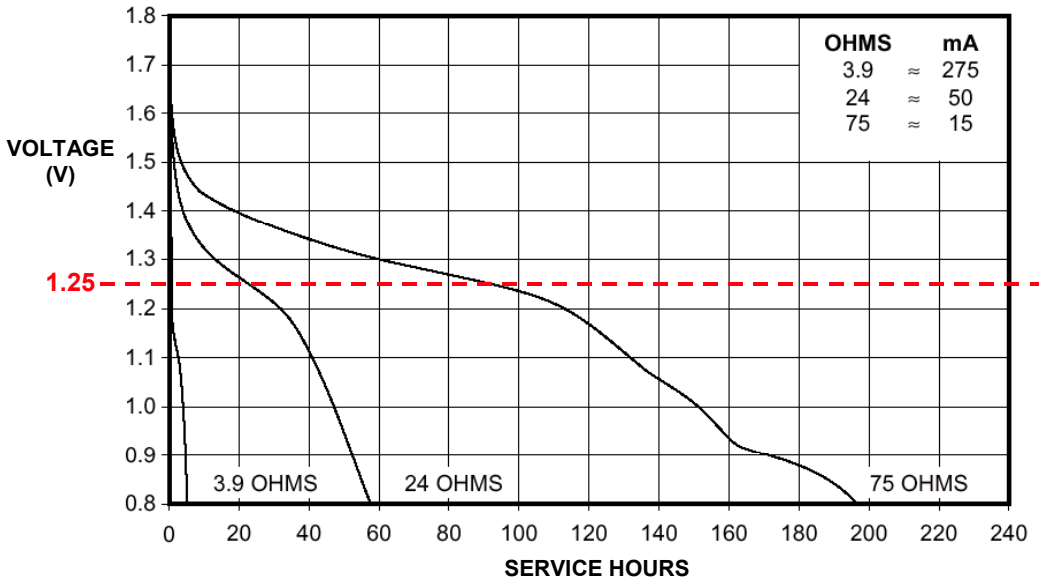
The strong interest in lower voltage DSPs is clearly visible in the shifting sales percentages for 5-V and 3.3-V parts. Sales growth for 3.3-V DSPs has increased at more than twice the rate of the rest of the DSP market (30% for all DSPs versus more than 70% for 3.3-V devices). This trend will continue as the high volume/high growth portable markets demand signal processors that contain all of the traits of the lower voltage DSPs.

On the one hand, the lower voltage ICs operate at lower power, allow smaller chip areas, and higher speeds. On the other hand, the lower voltage ICs must often interface to other ICs which operate at larger V_{DD} supply voltages thereby causing interface compatibility problems. Although lower operating voltages mean smaller signal swings, and hence less switching noise, noise margins are lower for low supply voltage ICs. A summary of key points relating to low voltage logic is summarized in Figure 9.154.

The popularity of 2.5-V devices can be partially explained by their ability to operate from two AA alkaline cells. Figure 9.155 shows the typical discharge characteristics for a AA cell under various load conditions (Reference 2). Note that at a load current of 15 mA, the voltage remains above +1.25 V (2.5 V for two cells in series) for nearly 100 hours. Therefore, an IC that can operate effectively at low currents with a supply voltage of 2.5 V ±10% (2.25 V - 2.75 V) is very useful in portable designs.

- **Lower Power for Portable Applications**
- **2.5V ICs Can Operate on Two "AA" Alkaline Cells**
- **Faster CMOS Processes, Smaller Geometries, Lower Breakdown Voltages**
- **Multiple Voltages in System: +5V, +3.3V, +2.5V, +1.8V DSP Core Voltage (VID), Analog Supply Voltage**
- **Interfaces Required Between Multiple Logic Types**
- **Lower Voltage Swings Produce Less Switching Noise**
- **Lower Noise Margins**
- **Less Headroom in Analog Circuits Decreases Signal Swings and Increases Sensitivity to Noise (But that's the subject of an entire seminar!)**

Figure 9.154: *Low Voltage Mixed-Signal ICs*



Courtesy: Duracell, Inc., Berkshire Corporate Park, Bethel, CT 06801
http://www.duracell.com

Figure 9.155: *Duracell MN1500 "AA" Alkaline Battery Discharge Characteristics*

In order to understand the compatibility issues relating to interfacing ICs operated at different V_{DD} supplies, it is useful to first look at the structure of a typical CMOS logic stage as shown in Figure 9.156.

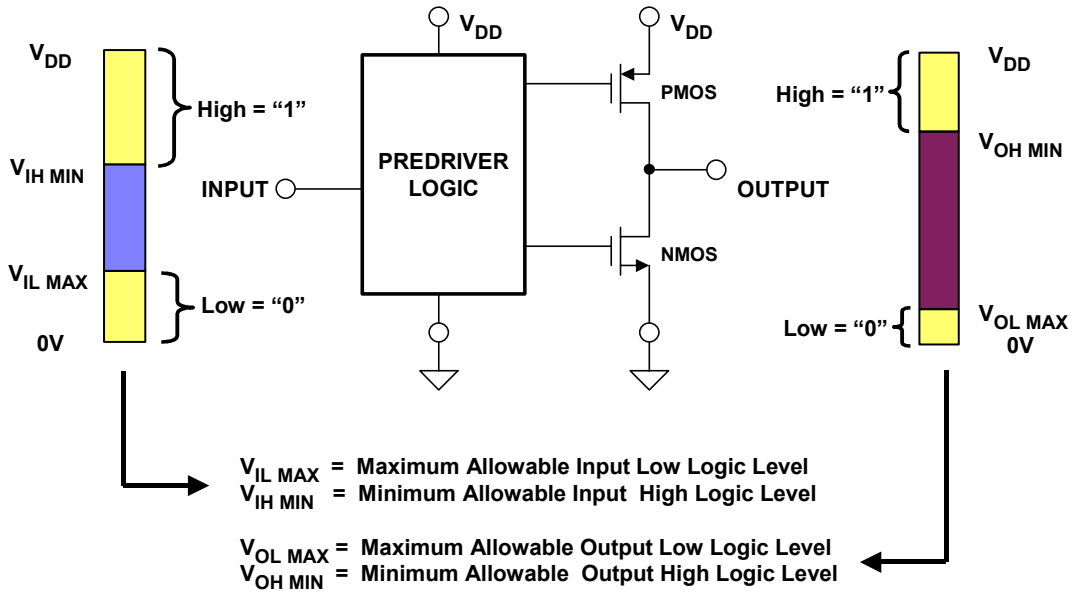


Figure 9.156: *Typical CMOS IC Output Driver Configuration*

Note that the output driver stage consists of a PMOS and an NMOS transistor. When the output is high, the PMOS transistor connects the output to the $+V_{DD}$ supply through its low on-resistance (R_{ON}), and the NMOS transistor is off. When the output is low, the NMOS transistor connects the output to ground through its on-resistance, and the PMOS transistor is off. The R_{ON} of a CMOS output stage can vary between 5 Ω and 50 Ω depending on the size of the transistors, which in turn, determines the output current drive capability.

A typical logic IC has its power supplies and grounds separated between the output drivers and the rest of the circuitry (including the pre-driver). This is done to maintain a clean power supply, which reduces the effect of noise and ground bounce on the I/O levels. This is increasingly important, since added tolerance and compliance are critical in I/O driver specifications, especially at low voltages.

Figure 9.156 also shows "bars" which define the minimum and maximum required input and output voltages to produce a valid high or low logic level. Note that for CMOS logic, the actual output logic levels are determined by the drive current and the R_{ON} of the transistors. For light loads, the output logic levels are very close to 0 V and $+V_{DD}$. The input logic thresholds, on the other hand, are determined by the input circuit of the IC.

There are three sections in the "input" bar. The bottom section shows the input range that is interpreted as a logic low. In the case of 5-V TTL, this range would be between 0 V and 0.8 V. The middle section shows the input voltage range where it is interpreted as neither a logic low nor a logic high. The upper section shows where an input is interpreted as a logic high. In the case of 5-V TTL, this would be between 2 V and 5 V.

Similarly, there are three sections in the "output" bar. The bottom range shows the allowable voltage for a logic low output. In the case of 5-V TTL, the IC must output a voltage between 0 V and 0.4 V. The middle section shows the voltage range that is not a

valid high or low—the device should never transmit a voltage level in this region except when transitioning from one level to the other. The upper section shows the allowable voltage range for a logic high output signal. For 5-V TTL, this voltage is between 2.4 V and 5 V. The chart does not reflect a 10% overshoot/undershoot also allowed on the inputs of the logic standard.

A summary of the existing logic standards using these definitions is shown in Figure 9.157. Note that the input thresholds of classic CMOS logic (series-4000, for example) are defined as 0.3 V_{DD} and 0.7 V_{DD}. However, most CMOS logic circuits in use today are compatible with TTL and LVTTL levels which are the dominant 5-V and 3.3-V operating standards for DSPs. Note that 5-V TTL and 3.3-V LVTTL input and output threshold voltages are identical. The difference is the upper range for the allowable high levels.

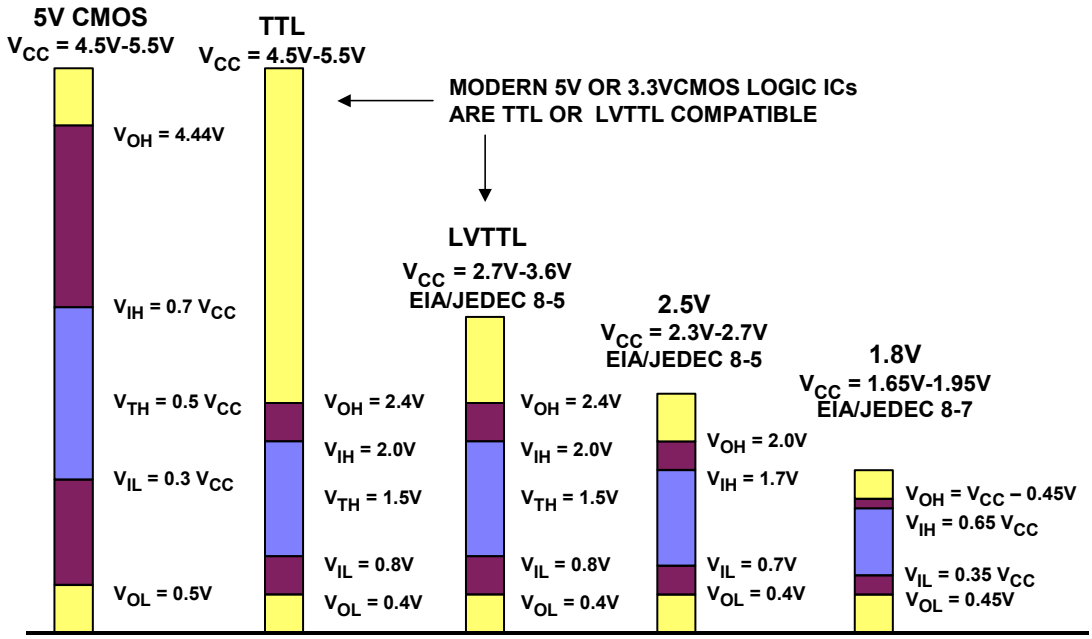


Figure 9.157: *Standard Logic Levels*

The international standards bureau JEDEC (Joint Electron Device Engineering Council) has created a 2.5-V standard (JEDEC standard 8-5) and a 1.8-V standard (Reference 3). There are also a wide range of other low voltage standards, such as GTL (Gunning Transceiver Logic), BTL (Backplane Transceiver Logic), ECL (Emitter-Coupled-Logic) PECL (Positive ECL Logic), and LVDS. However, most of these standards are aimed at application specific markets and not for general purpose semiconductor systems.

From this chart (Figure 9.157), it is possible to visualize some of the possible problems in connecting together two ICs operating on different standards. One example would be connecting a 5-V TTL device to a 3.3-V LVTTL IC. The 5-V TTL high level is too high for the LVTTL to handle (> 3.3V). This could cause permanent damage to the LVTTL chip. Another possible problem would be a system with a 2.5-V IC driving a 5-V CMOS device. The logic high level from the 2.5-V device is not high enough for it to register as a logic high on the 5-V CMOS input ($V_{IH\ MIN}$ = 3.5 V). These examples illustrate two possible types of logic level incompatibilities—either a device being driven with too high a voltage or a device not driving a voltage high enough for it to register a valid high logic

level with the receiving IC. These interfacing problems introduce two important concepts: *voltage tolerance* and *voltage compliance*.

Voltage Tolerance and Voltage Compliance

A device that is *voltage tolerant* can withstand a voltage greater than its V_{DD} on its I/O pins. For example, if a device has a V_{DD} of 2.5 V and can accept inputs equal to 3.3 V and can withstand 3.3 V on its outputs, the 2.5 V device is called 3.3 V tolerant. The meaning of *input* voltage tolerance is fairly obvious, but the meaning of *output* voltage tolerance requires some explanation. The output of a 2.5-V CMOS driver in the high state appears like a small resistor (R_{ON} of the PMOS FET) connected to 2.5 V. Obviously, connecting its output directly to 3.3 V is likely to destroy the device due to excessive current. However, if the 2.5-V device has a three-state output which is connected to a bus which is also driven by a 3.3-V IC, then the meaning becomes clearer. Even though the 2.5-V IC is in the off (third-state) condition, the 3.3-V IC can drive the bus voltage higher than 2.5 V, potentially causing damage to the 2.5-V IC output.

A device which is *voltage compliant* can receive signals from and transmit signals to a device which is operated at a voltage greater than its own V_{DD}. For example, if a device has a 2.5-V V_{DD} and can transmit and receive signals to and from a 3.3-V device, the 2.5-V device is said to be 3.3-V compliant.

The interface between the 5-V CMOS and 3.3-V LVTTL parts illustrates a lack of voltage tolerance; the LVTTL IC input is overdriven by the 5-V CMOS device output. The interface between the 2.5-V JEDEC and the 5-V CMOS part demonstrates a lack of voltage compliance; the output high level of the JEDEC IC does not comply to the input level requirement of a the 5-V CMOS device. The definitions of voltage compliance and voltage tolerance are repeated in Figure 9.158.

- **Voltage Tolerance:**
  - **A device that is *Voltage Tolerant* can *withstand* a voltage greater than its V_{DD} on its input and output pins. If a device has a V_{DD} of 2.5V and can accept inputs of 3.3V (±10%), the 2.5V device is 3.3V tolerant on its input. Input and output tolerance should be examined and specified separately.**

- **Voltage Compliance:**
  - **A device that is *Voltage Compliant* can *transmit and receive* signals to and from logic which is operated at a voltage greater than its own V_{DD}. If a device has a 2.5V V_{DD} and can properly transmit signals to and from 3.3V logic, the 2.5V device is 3.3V compliant. Input and output compliance should be examined and specified separately.**

Figure 9.158: *Logic Voltage Tolerance and Compatibility Definitions*

Interfacing 5V Systems to 3.3V Systems using NMOS FET "Bus Switches"

When combining ICs that operate on different voltage standards, one is often forced to add additional discrete elements to ensure voltage tolerance and compliance. In order to achieve voltage tolerance between 5-V and 3.3-V logic, for instance, a bus switch voltage translator such as the ADG3257 can be used (also see References 4, 5). The bus switch limits the voltage applied to an IC. This is done to avoid applying a larger input high voltage than the receiving device can tolerate.

As an example, it is possible to place a bus switch between a 5-V CMOS and 3.3-V LVTTL IC, and the two devices can then transmit data properly as shown in Figure 9.159. The bus switch is basically an NMOS FET. If 4.3 V is placed on the gate of the FET, the maximum passable signal is 3.3 V (approximately 1 V less than the gate voltage). If both input and output are below 3.3 V, the NMOS FET acts as a low resistance ($R_{ON} \approx 2\ \Omega$). As the input approaches 3.3 V, the FET on-resistance increases, thereby limiting the signal output. The ADG3257 is a quad 2:1 Mux/Demux bus switch with a gate drive enable as shown in the lower half of Figure 9.159. The V_{CC} of the ADG3257 sets the high level for the gate drive.

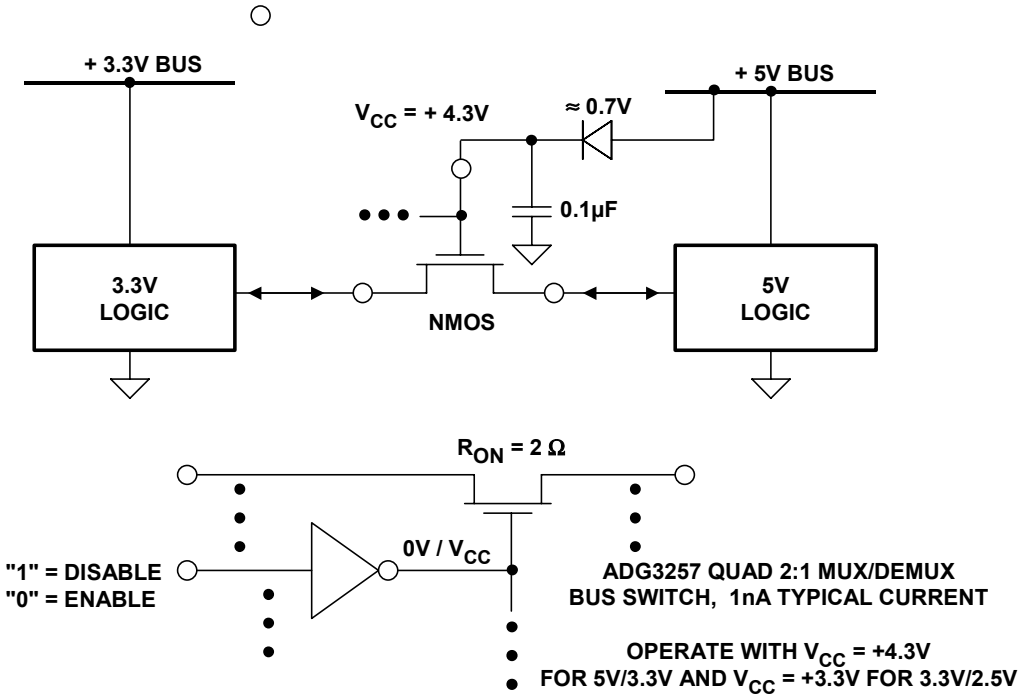


Figure 9.159: *+5 V/+3.3 V Bidirectional Interface Using NMOS FET Achieves Voltage Tolerance*

One way of creating a 4.3-V supply on a 5-V/3.3-V system board is to simply place a silicon diode between the 5-V supply and V_{CC} on the bus switch as shown in Figure 9.159. For 3.3 V/2.5 V applications, the V_{CC} pin can be connected directly to the +3.3-V supply. Some bus switches are designed to operate on either 3.3 V or 5 V directly and generate the internal gate bias level internally.

A bus switch removes voltage tolerance concerns in this mixed logic design. One convenient feature of bus switches is that they are bi-directional; this allows the designer to place a bus translator between two ICs and not have to create additional routing logic for input and output signals.

A bus switch increases the total power dissipation along with the total area required to layout a system. Since voltage bus switches are typically CMOS circuits, they have very low power dissipation ratings. An average value for added continuous power dissipation is 5 mW per package (10 switches), and this is independent of the frequency of signals which pass through the circuit. Bus switches typically have 8 - 20 I/O pins per package and take up approximately 25 to 50 mm^2 of board space.

One concern when adding interface logic into a circuit is a possible increase in propagation delay. Added propagation delay can create many timing problems in a design. Bus switches have very low propagation delay values.

The bus switch contributes practically no propagation delay (0.1 ns typical for the ADG3257) other than the RC delay of the typical R_{ON} of the switch and the load capacitance when driven by an ideal voltage source. Since the time constant is typically much smaller than the rise/fall times of typical driving signals, bus switches add very little propagation delay to the system. Low R_{ON} is therefore critical for bus switches, since the switch on-resistance in conjunction with the bus capacitance creates a single-pole filter which can add delay and reduce the maximum data rate. The typical on-capacitance of the ADG3257 is 10 pF, and this capacitance in conjunction with an R_{ON} of 4 Ω yields a rise/fall time of approximately 90 ps. Figure 9.160 shows the ADG3257 on-resistance as a function of input voltage for 5.5-, 5-, 4.5-, 3.3-, 3.0-, and 2.7-V supplies. Maximum pass voltage as a function of input voltage is shown in Figure 9.161.

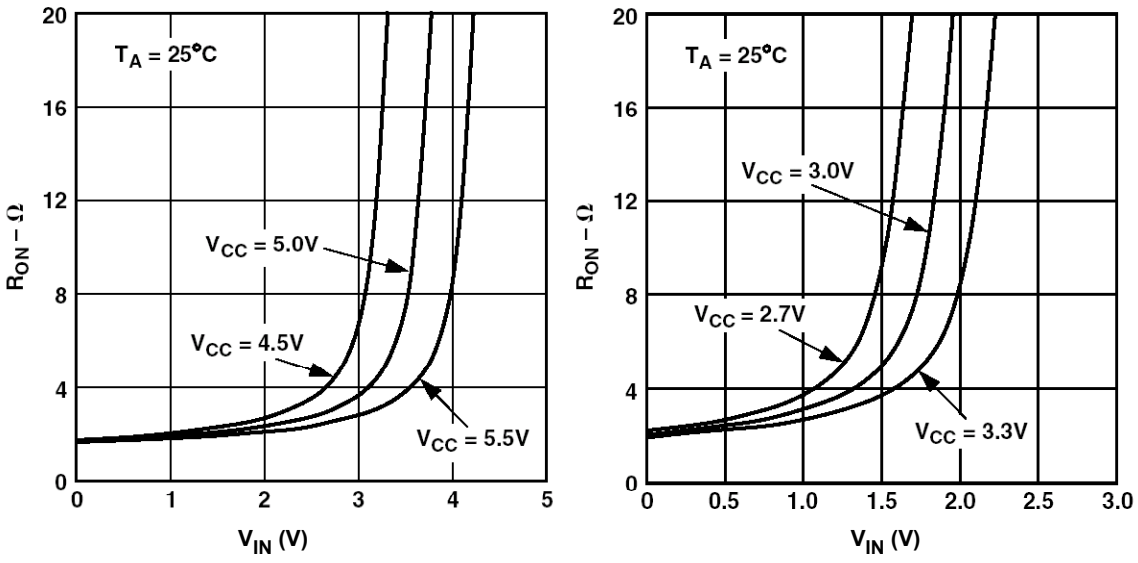


Figure 9.160: *ON Resistance vs. Input Voltage for ADG3257 Bus Switch*

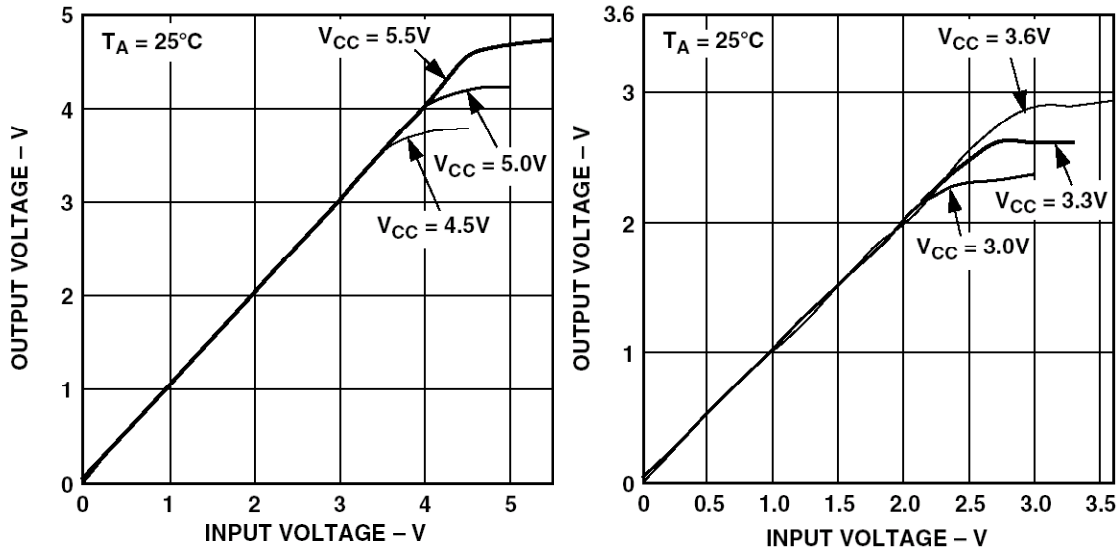


Figure 9.161: *Maximum Pass Voltage vs. Input Voltage for ADG3257 Bus Switch*

Eye diagrams for the ADG3257 operating at 622 Mbps and 933 Mbps are shown in Figure 9.162.

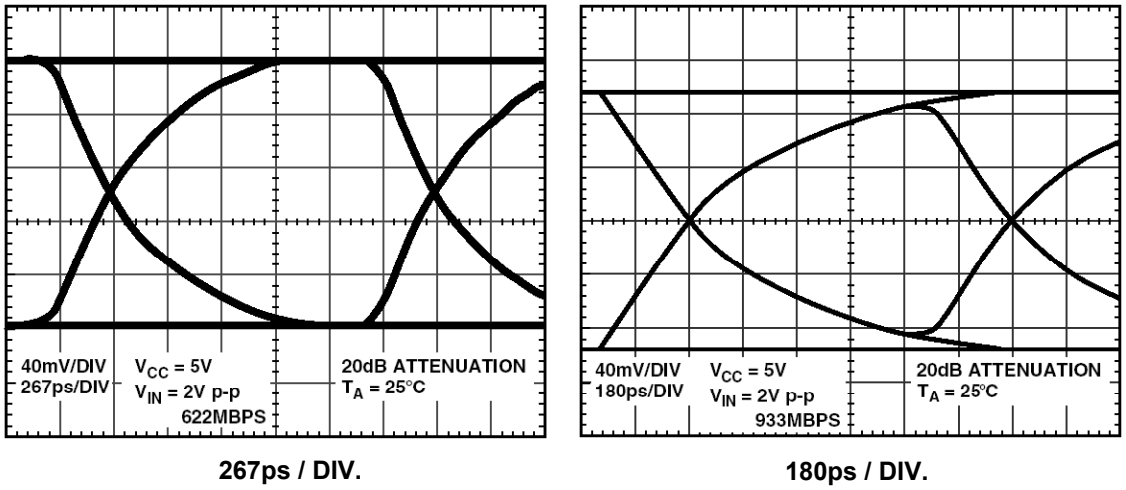


Figure 9.162: *Eye Diagrams for 622-Mbps and 933-Mbps Data Rates*

3.3V/2.5V Interfaces

Figure 9.163 shows two possibilities for a 3.3-V to 2.5-V logic interface. The top diagram (A) shows a direct connection. This will work provided the 2.5-V IC is 3.3-V tolerant on its input. If the 2.5-V IC is not 3.3-V tolerant, a low-voltage bus switch such as the ADG3231 can be used. In most cases, the connection between 3.3-V and 2.5-V systems can be bi-directional, even though the V_{OH} of 2.5-V logic is specified as +2.0 V which is

the same as the V_{IH} specification of 3.3-V logic (refer back to Figure 9.157). This point deserves further discussion.

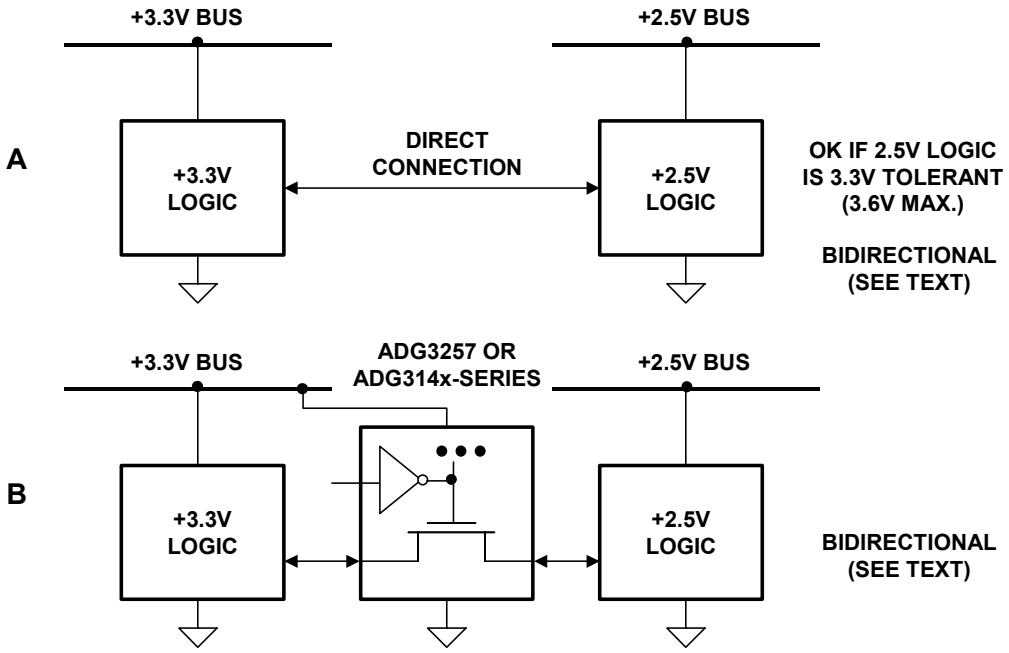


Figure 9.163: *+3.3-V to +2.5-V Interface*

Figure 9.164A shows a direct connection between 2.5-V and 3.3-V logic. In order for this to work, the 2.5-V output must be at least 2-V minimum per the JEDEC specifications. With no loading on the 2.5-V output, the 3.3-V IC input is connected directly to +2.5-V through the on-resistance of the PMOS transistor driver. This provides 0.5-V noise margin for the nominal supply voltage of 2.5 V. However, the tolerance on the 2.5-V bus allows it to drop to a minimum of 2.3 V, and the noise margin is reduced to 0.3 V. This may still work in a relatively quiet environment, but could be marginal if there is noise on the supply voltages.

Adding a 1.6-kΩ pull-up resistor as shown in Figure 9.164B ensures the 2.5-V output will not drop below 2.5 V due to the input current of the 3.3-V device, but the degraded noise margin still exists for a 2.3-V supply. With a 50% duty cycle, the resistor adds about 3.4-mW power dissipation per output.

A more reliable interface between 2.5-V and 3.3-V logic is shown in Figure 9.164C, where a logic translator such as the ADG3231 is used. This solves all noise margin problems associated with (A) and (B) and requires about 2-µA maximum per output.

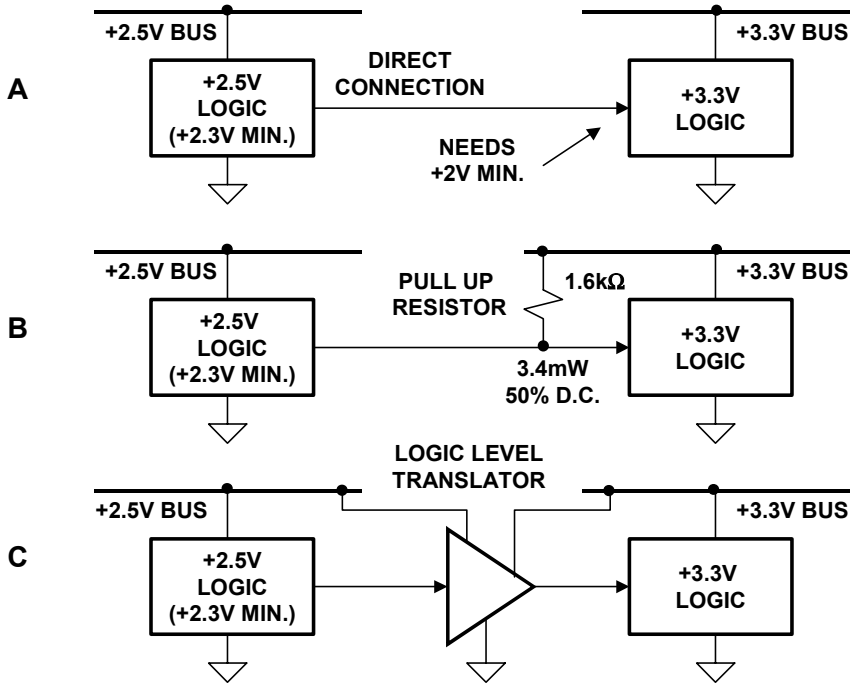


Figure 9.164: *+2.5-V to +3.3-V Interface Analyzed*

3.3V/2.5V, 3.3V/1.8V, 2.5V/1.8V Interfaces

The ADG3241, ADG3242, ADG3243, ADG3245, ADG3246, ADG3247, ADG3248, and ADG3249 are low voltage bus switches optimized for operation on 3.3-V or 2.5-V supplies. The family includes 1-, 2-, 8-, 10- and dual 8-bit switches, all of which are 2-port switches. The ADG3241, ADG3242, ADG3245, ADG3246, ADG3247, and ADG3249 have 2.5-V or 1.8-V selectable level shift capability. The family offers a fast, low-power solution for 3.3-/2.5-V, 3.3-/1.8-V, and 2.5-/1.8-V unidirectional interfaces. Figure 9.165 shows the ADG32xx-family used as 3.3-/1.8-V level shifters and 2.5-/1.8-V shifters.

Translating from 1.8 V to 2.5 V, 1.8 V to 3.3 V, (and sometimes 2.5 V to 3.3 V as previously discussed) requires a logic translator such as the ADG3231 shown in Figure 9.166. The two voltage buses can be any value between 1.65 V and 3.6 V. The ADG3231 is a single-channel translator in a SOT-23 package, and the ADG3232 is a 2:1 multiplexer/level translator also in a SOT-23 package.

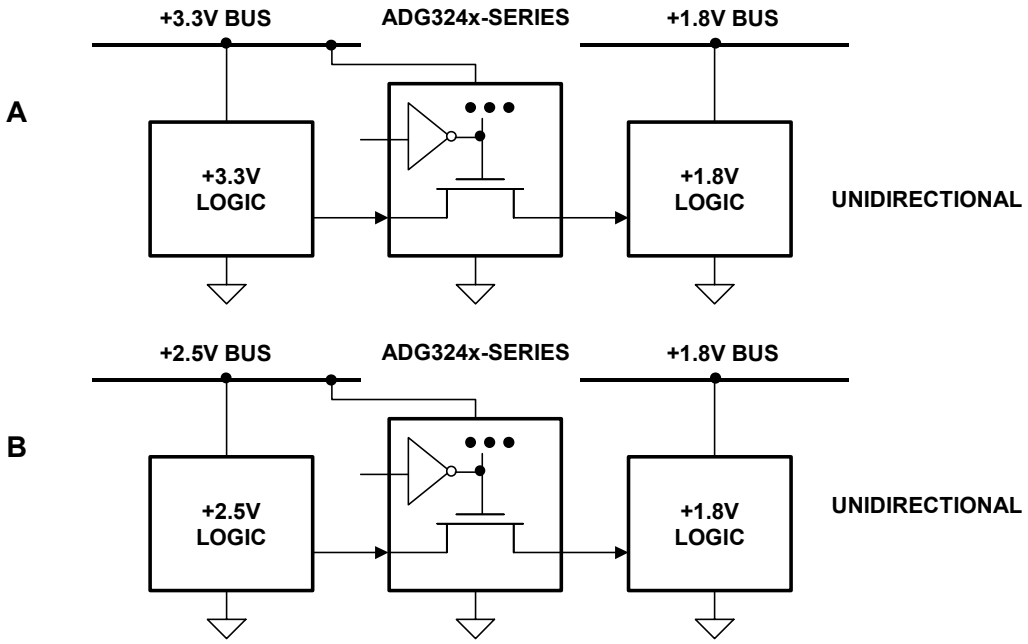


Figure 9.165: *+3.3 V to +1.8 V, 2.5 V to +1.8 V Unidirectional Interfaces*

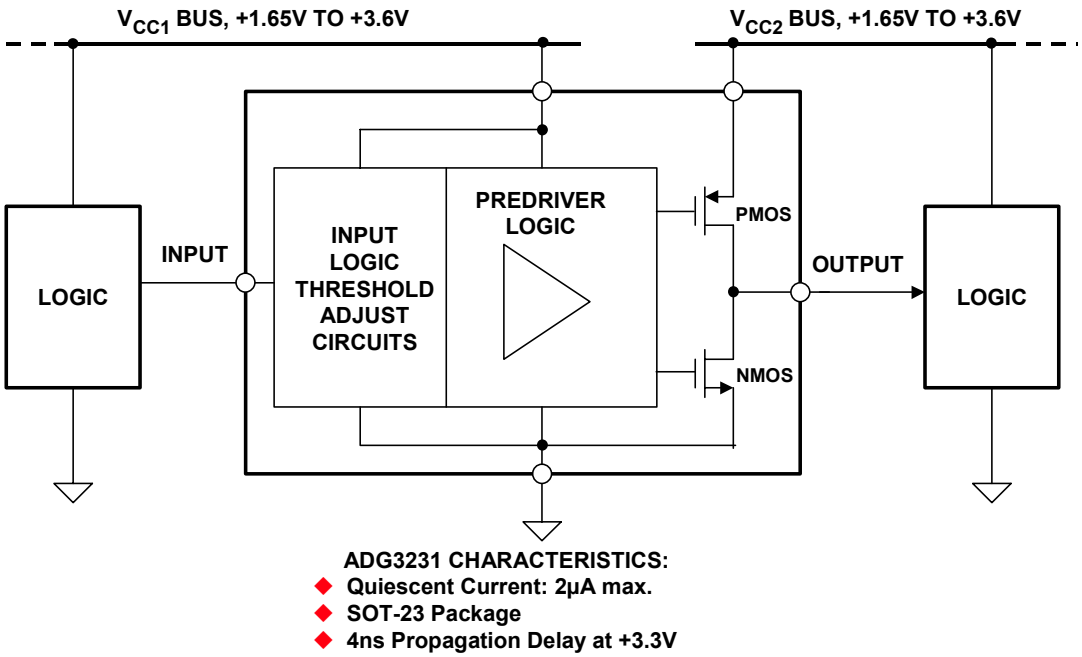


Figure 9.166: *ADG3231 Low Voltage Logic Level Translator*

The ADG3233 is a bypass switch designed on a submicron process that operates from supplies as low as 1.65 V. The device is guaranteed for operation over the supply range 1.65 V to 3.6 V. It operates from two supply voltages, allowing bidirectional level translation, i.e., it translates low voltages to higher voltages and vice versa. The signal path is unidirectional, meaning data may only flow from A to Y. This type of device may be used in applications that require a bypassing function. It is ideally suited to bypassing devices in a JTAG chain or in a daisy-chain loop. One switch could be used for each

device or a number of devices, thus allowing easy bypassing of one or more devices in a chain. This may be particularly useful in reducing the time overhead in testing devices in the JTAG chain or in daisy-chain applications where the user does not wish to change the settings of a particular device.

The bypass switch is packaged in two of the smallest footprints available for its required pin count. The 8-lead SOT-23 package requires only 8.26 mm × 8.26 mm board space, while the MSOP package occupies approximately 15 mm × 15 mm board area. A functional block diagram of the ADG3233 is shown in Figure 9.167.

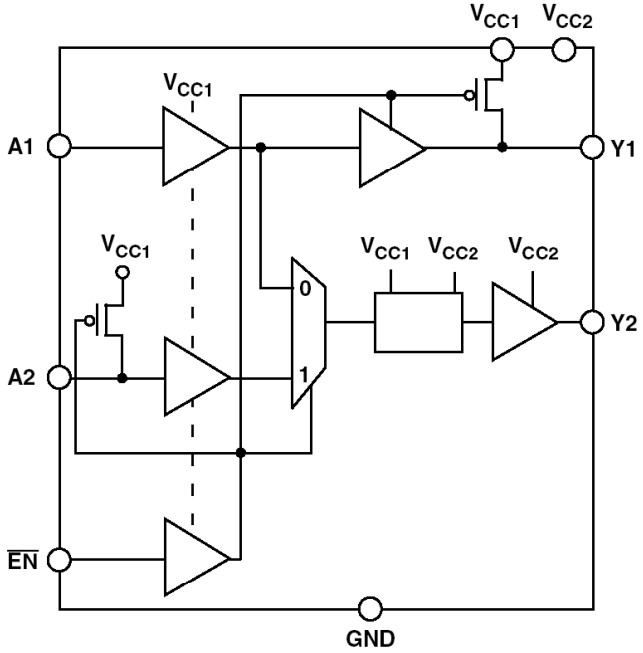


Figure 9.167: *ADG3233 Low Voltage 1.65-V to 3.6-V, Logic Level Translator and Bypass Switch*

Figure 9.168 shows the bypass switch being used in normal mode. In this mode, the signal paths are from A1 to Y1 and A2 to Y2. The device will level translate the signal applied to A1 to a V_{CC1} logic level (this level translation can be either to a higher or lower supply) and route the signal to the Y1 output, which will have standard V_{OL}/V_{OH} levels for V_{CC1} supplies. The signal is then passed through Device 1 and back to the A2 input pin of the bypass switch. The logic level inputs of A2 are with respect to the V_{CC1} supply. The signal will be level translated from V_{CC1} to V_{CC2} and routed to the Y2 output pin of the bypass switch. Y2 output logic levels are with respect to the V_{CC2} supply.

Figure 9.169 illustrates the device as used in bypass operation. The signal path is now from A1 directly to Y2, thus bypassing Device 1 completely. The signal will be level translated to a V_{CC2} logic level and available on Y2, where it may be applied directly to the input of Device 2. In bypass mode, Y1 is pulled up to V_{CC1}. The three supplies in Figures 9.168 and 9.169 may be any combination of supplies, i.e., V_{CC0}, V_{CC1}, and V_{CC2} may be any combination of supplies, for example, 1.8 V, 2.5 V, and 3.3 V.

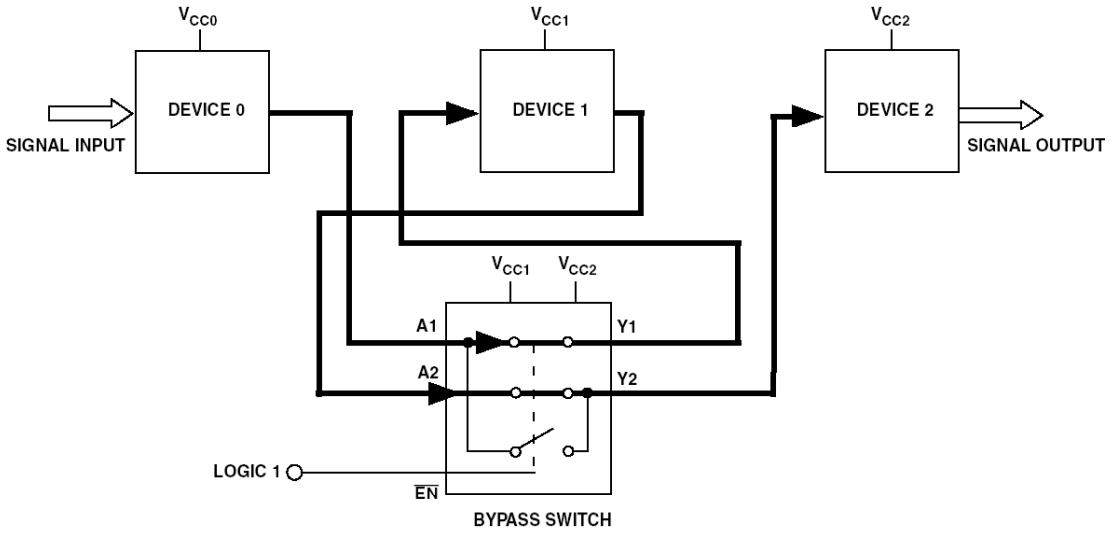


Figure 9.168: *ADG3233 Bypass Switch in Normal Mode*

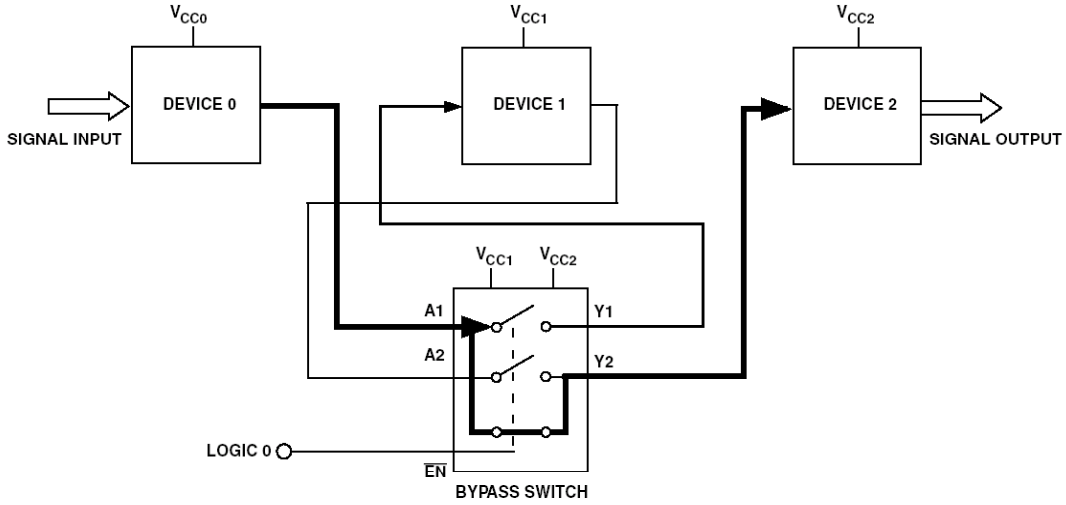


Figure 9.169: *ADG3233 Bypass Switch in Bypass Mode*

Hot Swap and Hot Plug Applications of Bus Switches

Hot swapping is adding and/or removing plug-in circuitry in a system with the power on (see Reference 8). Examples of applications that require the ability to hot swap are docking stations for laptops and line cards for telecommunications switches. During a hot swap event, the connectors on the back plane are "live"; the add-on card must be able to cope with this condition. If the bus can be isolated prior to insertion, one has more control over the hot-swap event. Isolation can be achieved using a digital switch, ideally positioned on the add-on card between the connector and the device (Figure 9.170). However, it is important that the ground pin of the add-on card connect to the ground pin of the back plane before any other signal or power pins, and it must be the last to disconnect when a card is removed.

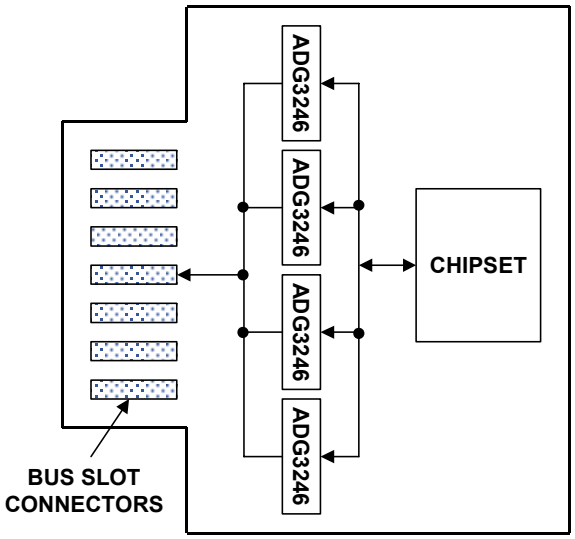


Figure 9.170: *Hot Swapping with the ADG3246 Bus Switch*

Critical systems, such as ADSL (Asynchronous Digital Subscriber Line), manufacturing controls, servers, and airline reservations must not be shut down. If new hardware, such as a plug-in modem, needs to be added to the system, it has to be done while the system is up and running. This process of adding hardware during mandatory continuous operation is known as hot plug (see Reference 9). To ensure smooth execution of the process, a digital switch can be wired between the connector and the internal bus (Figure 9.171). During the hot-plug event, the switch is turned off to provide isolation of the specific circuit location.

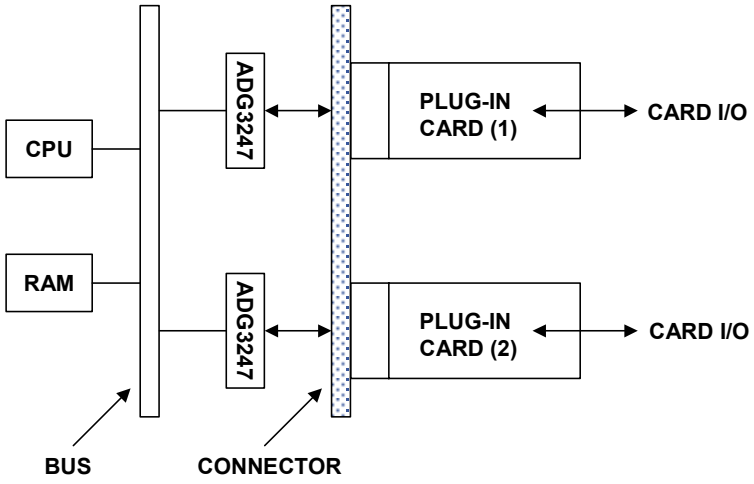


Figure 9.171: *Using the ADG3247 in a Hot-Plug Application*

Internally Created Voltage Tolerance / Compliance

Modern high performance CMOS DSPs and microprocessors typically operate on core voltages between 1 V and 2 V. These low voltages yield optimum speed-power performance. However, the logic levels in the core are not compatible with standard 2.5-V or 3.3-V I/O interfaces. This problem is typically solved as shown in Figure 9.172, where the logic core operates at a reduced voltage, but the output drivers operate at a standard supply voltage level of 2.5 V or 3.3 V.

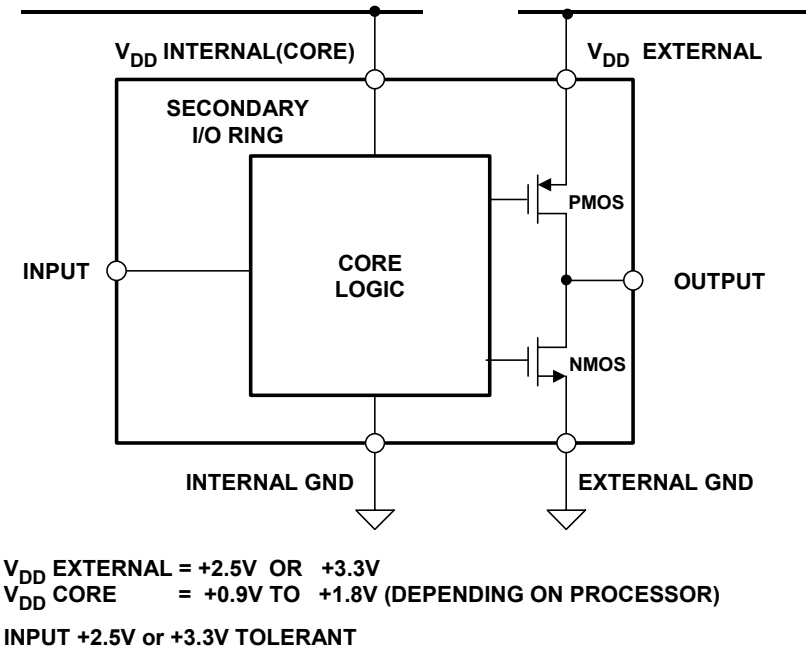


Figure 9.172: *Internal Compliance and Tolerance in a CMOS IC With Secondary I/O Ring*

The technique followed by many IC manufacturers is to provide a secondary I/O ring, i.e., the I/O drivers are driven by the 2.5-V or 3.3-V power supply, hence the device is compatible with 2.5-V or 3.3-V logic levels. Note that the inputs must be compliant and tolerant to the I/O supply voltage. There are several issues to consider in a dual-supply logic IC design of this type:

- *Power-Up Sequencing*: If two power supplies are required to give an IC additional tolerance / compliance, what is the power-up sequence? Is it a requirement that the power supplies are switched on simultaneously or can the device only have a voltage supplied on the core or only on the I/O ring? This problem can be easily solved if the core voltage is generated from the I/O supply voltage using a low dropout linear regulator.

- *Process Support and Electro-Static Discharge (ESD) Protection*: The transistors created in the IC's fabrication process must be able to both withstand and drive high voltages. The high voltage transistors create additional fabrication costs since they require more processing steps to build in high voltage tolerance. Designs with standard transistors require additional circuitry. The I/O drivers must also provide

ESD protection for the device. Most current designs limit the overvoltage to below one diode drop (0.7 V) above the power supply. Protection for larger overvoltage requires more diodes in series.

- *Internal High Voltage Generation*: The PMOS transistors need to be placed in a substrate well which is tied to the highest on-chip voltage to prevent lateral diodes from turning on and drawing excessive current. This high voltage can either be generated on chip using charge pumps or from an external supply. This requirement can make the design complex, since one cannot efficiently use charge pumps to generate higher voltages and also achieve low standby current. In most cases, the voltage is supplied externally.

- *Chip Area*: Die size is a primary factor in reducing costs and increasing yields. Tolerance and compliance circuitry may require either more or larger I/O devices to achieve the desired performance levels.

- *Testing*: Since the core and the I/O can be at different voltages, testing the device for all possible combinations of voltages can be complicated, adding to the total cost of the IC.

REFERENCES:
9.7 LOW VOLTAGE LOGIC INTERFACING

1. P. Alfke, *Low-Voltage FPGAs Allow 3.3V/5V System Design*, **Electronic Design**, p. 70-76, August 18, 1997.

2. AA Alkaline Battery Discharge Characteristics, Duracell Inc., Berkshire Corporate Park, Bethel, CT 06801, http://www.duracell.com

3. Joint Electron Device Engineering Council (JEDEC), http://www.jedec.org, Standard JESD8-5, October 1995, and Standard JESD8-7, February, 1997,

4. QS3384 Data Sheet, Integrated Device Technology (IDT), Inc., 2975 Stender Way, Santa Clara, CA 95054, http://www.idt.com

5. Pericom Semiconductor Corporation, 2380 Bering Drive, San Jose, CA 95131, http://www.pericom.com

6. H. Johnson, M. Graham, **High Speed Digital Design**, Prentice Hall, 1993.

7. Eva Murphy and Catherine Redmond, "Bus Switches for Speed, Safety, and Efficiency: What They Are and What You Should Know about Them," **Analog Dialogue** 36-06, Analog Devices, Inc., 2002.

8. Compact PCI Hot Swap Specification R1.0.

9. PCI Hot-Plug Specification R1.0, October 6, 1997.

NOTES:

SECTION 9.8: BREADBOARDING AND PROTOTYPING

Walt Kester, James Bryant, Walt Jung

A basic principle of a breadboard or a prototype structure is that it is a *temporary* one, designed to test the performance of an electronic circuit or system. By definition it must therefore be easy to modify, particularly so for a breadboard.

There are many commercial prototyping systems, but unfortunately for the analog designer, almost all of them are designed for prototyping *digital* systems. In such environments, noise immunities are hundreds of millivolts or more. Prototyping methods commonly used include non copper-clad Matrix board, Vectorboard, wire-wrap, and plug-in breadboard systems. Quite simply, these all are unsuitable for high performance or high frequency analog prototyping, because of their excessively high parasitic resistance, inductance, and capacitance levels. Even the use of standard IC sockets is inadvisable in many prototyping applications (more on this, below).

- **Always Use a Large Area Ground Plane for Precision or High Frequency Circuits**
- **Minimize Parasitic Resistance, Capacitance, and Inductance**
- **If Sockets Are Required, Use "Pin Sockets" ("Cage Jacks")**
- **Pay Equal Attention to Signal Routing, Component Placement, Grounding, and Decoupling in Both the Prototype and the Final Design**
- **Popular Prototyping Techniques:**
  - **Freehand "Deadbug" Using Point-to-point Wiring**
  - **"Solder-mount"**
  - **Milled PC Board From CAD Layout**
  - **Multilayer Boards: Double-sided With Additional Point-to-point Wiring**
- **Modern Surface-Mount ICs in Small Packages Require Special Techniques—Usually a Preliminary Multilayer PC Board Layout**

Figure 9.173: *A Summary of Analog Prototyping System Key Points*

Figure 9.173 summarizes a number of key points on selecting a useful analog breadboard and/or prototyping system, which are further discussed below.

One of the more important considerations in selecting a prototyping method is the requirement for a large-area ground plane. This is required for high frequency circuits as well as low speed precision circuits, especially when prototyping circuits involving ADCs or DACs. The differentiation between *high-speed* and *high-precision* mixed-signal circuits is difficult to make. For example, 16+ bit ADCs (and DACs) may operate on high speed clocks (>10 MHz) with rise and fall times of less than a few nanoseconds, while the effective throughput rate of the converters may be less than 100 kSPS. Successful

prototyping of these circuits requires that equal (and thorough) attention be given to good high-speed and high-precision circuit techniques.

Several years ago, many ICs were offered in both DIP and surface-mount packages, so breadboarding and prototyping could be done using the user-friendly DIP package. Today, however, most high-performance data converters are not available in DIP packages—and if they were, the added package parasitics would limit performance in many cases.

Breadboarding and prototyping in today's environment is especially difficult, because modern surface-mounted ICs in small packages can be extremely difficult to solder into any type of PC board using manual techniques. Ball grid array (BGA) packages are nearly impossible to solder manually. Sockets—very expensive if available—are generally out of the question because of added parasitics, so in many cases, an actual multilayer PC board must be designed and fabricated. This trend has placed an even greater responsibility on the IC manufacturer to supply a variety of high quality well documented evaluation boards to assist in the initial design phases of a project.

"Deadbug" Prototyping

A simple technique for analog prototyping where DIP ICs are available uses a solid copper-clad board as a ground plane (see References 1 and 2). In this method, the ground pins of the ICs are soldered directly to the plane, and the other components are wired together above it. This allows HF decoupling paths to be very short indeed. All lead lengths should be as short as possible, and signal routing should separate high-level and low-level signals. Connection wires should be located close to the surface of the board to minimize the possibility of stray inductive coupling. In most cases, 18-gauge or larger insulated wire should be used. Parallel runs should not be "bundled" because of possible coupling. Ideally the layout (at least the relative placement of the components on the board) should be similar to the layout to be used on the final PCB. This approach is often referred to as *deadbug* prototyping, because the ICs are often mounted upside down with their leads up in the air (with the exception of the ground pins, which are bent over and soldered directly to the ground plane). The upside-down ICs look like deceased insects, hence the name.

Figure 9.174 shows a hand-wired "deadbug" analog breadboard. This circuit uses two high speed op amps, and in fact gives excellent performance in spite of its lack of esthetic appeal. The IC op amps are mounted upside down on the copper board with the leads bent over. The signals are connected with short point-to-point wiring. The characteristic impedance of a wire over a ground plane is about 120 Ω, although this may vary as much as ±40% depending on the distance from the plane. The decoupling capacitors are connected directly from the op amp power pins to the copper-clad ground plane. When working at frequencies of several hundred MHz, it is a good idea to use only one side of the board for ground. Many people drill holes in the board and connect the sides together by soldering short pieces of wire. If care isn’t taken, this may result in unexpected ground loops between the two sides of the board, especially at RF frequencies.

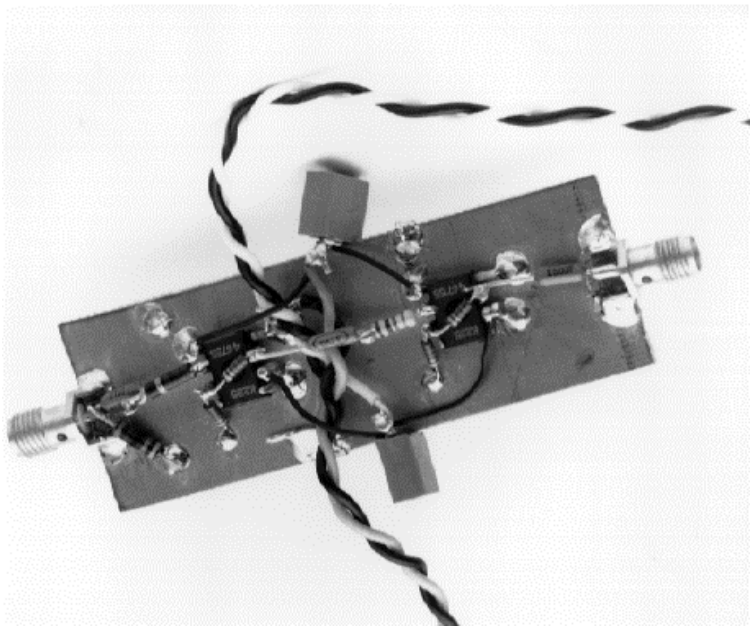


Figure 9.174: *A "Deadbug" Analog Breadboard*

Pieces of copper-clad board may be soldered at right angles to the main ground plane to provide screening, or circuitry may be constructed on both sides of the board (with through-hole connections) with the board itself providing screening. For this, the board will need corner standoffs to protect underside components from being crushed.

When the components of a breadboard of this type are wired point-to-point in the air (a type of construction strongly advocated by Bob Pease (see Reference 2) and sometimes known as "bird's nest" construction) there is always the risk of the circuitry being crushed and resulting short-circuits. Also, if the circuitry rises high above the ground plane, the screening effect of the ground plane is diminished, and interaction between different parts of the circuit is more likely. Nevertheless, the technique is very practical and widely used because the circuit may easily be modified (this of course assumes the person doing the modifications is adept with soldering techniques).

Another prototype breadboard variation is shown in Figure 9.175. Here the single-sided copper-clad board has pre-drilled holes on 0.1" centers (see Reference 3). Power busses are used at the top and bottom of the board. The decoupling capacitors are used on the power pins of each IC. Because of the loss of copper area due to the pre-drilled holes, this technique does not provide as low a ground impedance as a completely covered copper-clad board of Figure 9.174, so be forewarned.

In a variation of this technique, the ICs and other components are mounted on the non-copper-clad side of the board. The holes are used as vias, and the point-to-point wiring is done on the copper-clad side of the board. Note that the copper surrounding each hole used for a via must be drilled out, to prevent shorting. This approach requires that all IC

pins be on 0.1" centers. For low frequency circuits, low profile sockets can be used, and the socket pins then will allow easy point-to-point wiring.

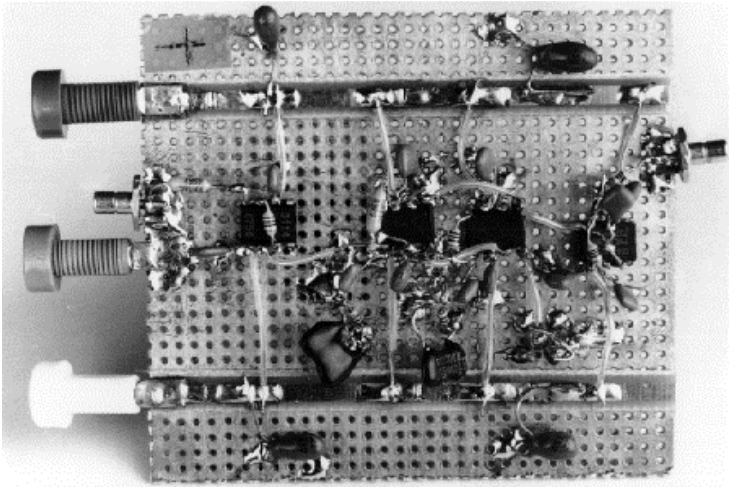


Figure 9.175: *"A Deadbug" Prototype Using 0.1" Pre-Drilled Single-Sided, Copper-Clad Printed Board Material*

Solder-Mount Prototyping

There is a commercial breadboarding system which has most of the advantages of the above techniques (robust ground, screening, ease of circuit alteration, low capacitance and low inductance) and several additional advantages: it is rigid, components are close to the ground plane, and where necessary, node capacitances and line impedances can be calculated easily. This system is made by Wainwright Instruments and is available in Europe as "Mini-Mount" and in the USA (where the trademark "Mini-Mount" is the property of another company) as "Solder-Mount" (see References 4 and 5).

Solder-Mount consists of small pieces of PCB with etched patterns on one side and contact adhesive on the other. These pieces are stuck to the ground plane, and components are soldered to them. They are available in a wide variety of patterns, including ready-made pads for IC packages of all sizes from 8-pin SOICs to 64-pin DILs, strips with solder pads at intervals (which intervals range from 0.040" to 0.25", the range includes strips with 0.1" pad spacing which may be used to mount DIL devices), strips with conductors of the correct width to form microstrip transmission lines (50 Ω, 60 Ω, 75 Ω or 100 Ω) when mounted on the ground plane, and a variety of pads for mounting various other components. Self-adhesive tinned copper strips and rectangles (LO-PADS) are also available as tie-points for connections. They have a relatively high capacitance to ground and therefore serve as low-inductance decoupling capacitors. They come in sheet form and may be cut with a knife or scissors.

The main advantage of Solder-Mount construction over "bird's nest" or "deadbug" is that the resulting circuit is far more rigid, and, if desired, may be made far smaller (the latest Solder-Mounts are for surface-mount devices and allow the construction of breadboards scarcely larger than the final PCB, although it is generally more convenient if the prototype is somewhat larger). Solder-Mount is sufficiently durable that it may be used for small quantity production as well as prototyping.

Figure 9.176 shows an example of a 2.5-GHz phase-locked-loop prototype, built with Solder-Mount techniques. While this is a high speed circuit, the method is equally suitable for the construction of high resolution low frequency analog circuitry.

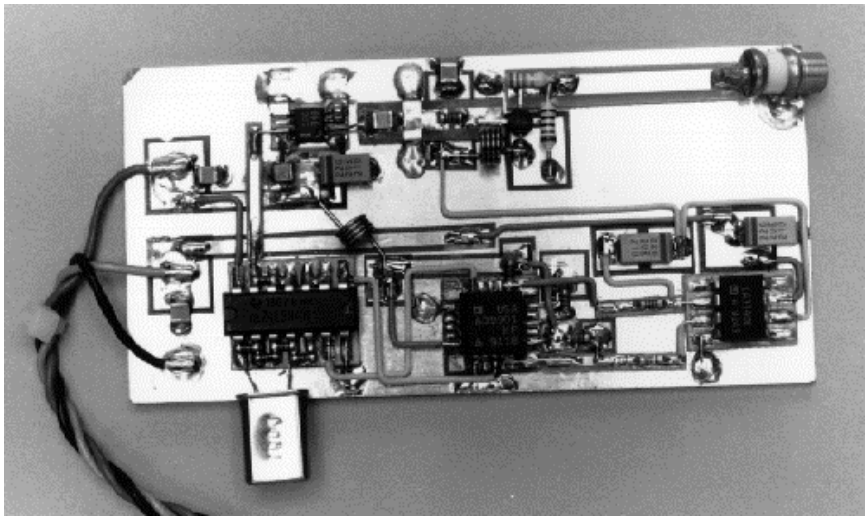


Figure 9.176: *A "Solder-Mount" Constructed Prototype Board*

A particularly convenient feature of Solder-Mount at VHF is the relative ease with which transmission lines can be formed. As noted earlier, if a conductor runs over a ground plane, it forms a microstrip transmission line. The Solder-Mount components include strips which form microstrip lines when mounted on a ground plane (they are available with impedances of 50 Ω, 60 Ω, 75 Ω, and 100 Ω). These strips may be used as transmission lines for impedance matching, or alternately, more simply as power buses. Note that glass fiber/epoxy PCB is somewhat lossy at VHF/ UHF, but losses will probably be tolerable if microstrip runs are short.

Milled PCB Prototyping

Both "deadbug" and "Solder-Mount" prototypes become tedious for complex analog circuits, and larger circuits are better prototyped using more formal layout techniques.

There is a prototyping approach that is but one step removed from conventional PCB construction, described as follows. This is to actually lay out a double-sided board, using conventional CAD techniques. PC-based software layout packages offer ease of layout as well as schematic capture to verify connections (see References 6 and 7). Although most layout software has some degree of auto-routing capability, this feature is best left to digital designs. The analog traces and component placements should be done by hand, following the rules discussed elsewhere in this chapter. After the board layout is complete, the software verifies the connections per the schematic diagram net list.

Many designers find that they can make use of CAD techniques to lay out simple boards. The result is a pattern-generation tape (or Gerber file) which would normally be sent to a PCB manufacturing facility where the final board is made.

Rather than use a PCB manufacturer, however, automatic drilling and milling machines are available which accept the PG tape directly (see References 8 and 9). An example of such a prototype circuit board is shown in Figure 9.177 (top view).

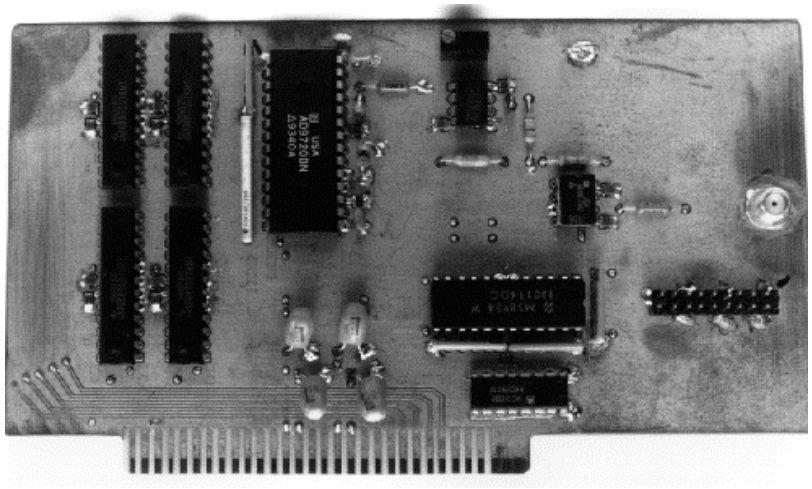


Figure 9.177: *A Milled Circuit Construction Prototype Board (Top View)*

These systems produce either single or double-sided circuit boards directly, by drilling all holes and using a milling technique to remove conductive copper, thus creating the required insulation paths, and finally, the finished prototype circuit board. The result can be a board functionally quite similar to a final manufactured double-sided PCB.

However, it should be noted that a chief caveat of this method is that there is no "plated-through" hole capability. Because of this, any conductive "vias" required between the two layers of the board must be manually wired and soldered on both sides.

Minimum trace widths of 25 mils (1 mil = 0.001") and 12 mil spacing between traces are standard, although smaller trace widths can be achieved with care. The minimum spacing between lines is dictated by the size of the milling bit used, typically 10 to 12 mils.

A bottom-side view of this same milled prototype circuit board is shown in Figure 9.178. The accessible nature of the copper pattern allows access to the traces for modifications.

Perhaps the greatest single advantage of the milled circuit type of prototype circuit board is that it approaches the format of the final PCB design most closely. By its very nature

however, it is basically limited to only single or double-sided boards—rendering it virtually useless for surface-mount designs.

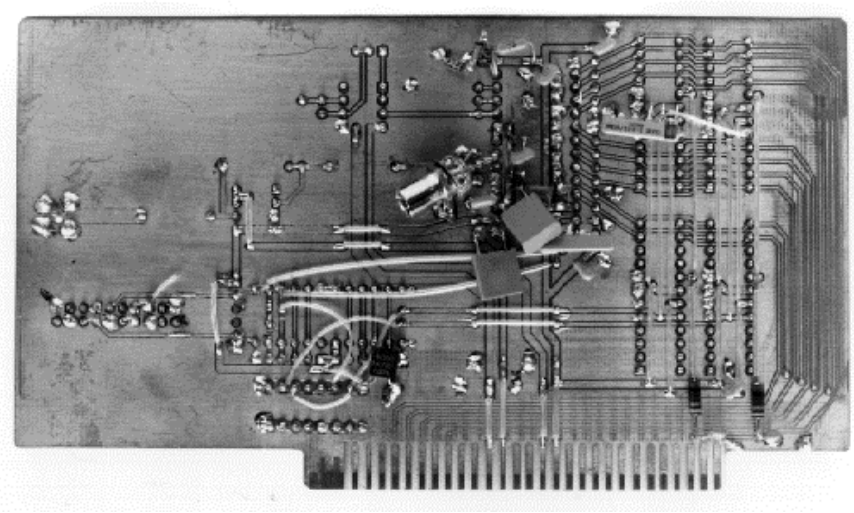


Figure 9.178: *A Milled Circuit Construction Prototype Board (Bottom View)*

Beware of Sockets!

IC sockets can degrade the performance of high speed or high precision analog ICs. Although they make prototyping easier, even *low-profile* sockets often introduce enough parasitic capacitance and inductance to degrade the performance of a high speed circuit. If sockets must be used, a socket made of individual *pin sockets* (sometimes called *cage jacks*) mounted in the ground plane board may be acceptable, as in Figure 9.179.

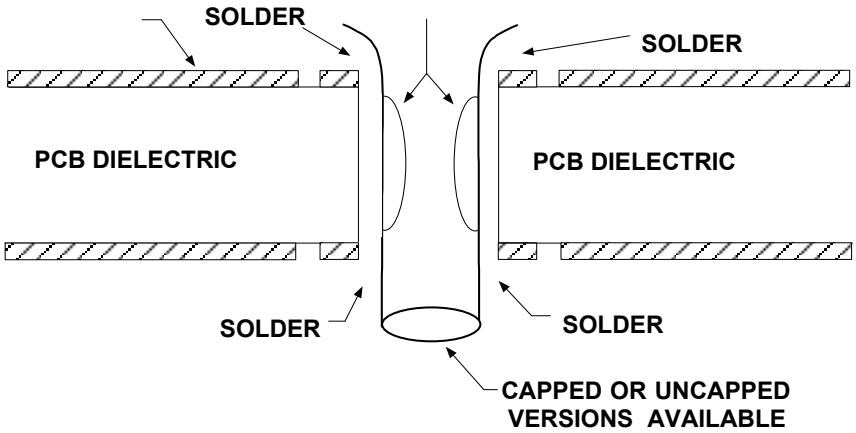


Figure 9.179: *When Necessary, Use Pin Sockets for Minimal Parasitic Effects*

To use this technique, clear the copper (on both sides of the board) for about 0.5-mm around each ungrounded pin socket, Then solder the grounded socket pins to ground, on both sides of the board.

Both capped and uncapped versions of these pin sockets are available (AMP part numbers 5-330808-3, and 5-330808-6, respectively). The pin sockets protrude through the board far enough to allow point-to-point wiring interconnections.

Because of the spring-loaded gold-plated contacts within the pin socket, there is good electrical and mechanical connection to the IC pins. Multiple insertions, however, may degrade the performance of the pin socket, so this factor should be kept in mind.

Note also that the uncapped versions allow the IC pins to extend out the bottom of the socket. This feature leads to an additional useful function. Once a prototype using the pin sockets is working and no further changes are to be made the IC pins can be soldered directly to the bottom of the socket. This establishes a rugged, permanent connection.

Some Additional Prototyping Points

The prototyping techniques discussed so far have been limited to single or double-sided PCBs. Multilayer PCBs do not easily lend themselves to standard prototyping techniques. If multilayer board prototyping is required, one side of a double-sided board can be used for ground and the other side for power and signals. Point-to-point wiring can be used for additional runs which would normally be placed on the additional layers provided by a multi-layer board. However, it is difficult to control the impedance of the point-to-point wiring runs, and the high frequency performance of a circuit prototyped in this manner may differ significantly from the final multilayer board.

Other difficulties in prototyping may occur with op amps or other linear devices having bandwidths greater than a few hundred megahertz. Small variations in parasitic capacitance (< 1 pF) between the prototype and the final board can cause subtle differences in bandwidth and settling time.

Sometimes, prototyping is done with DIP packages (if available), when the final production package is an SOIC. *This is not recommended!* At high frequencies, small package-related parasitic differences can account for different performance, between prototype and final PCB. To minimize this effect, always prototype with the final packages.

Evaluation Boards

Most manufacturers of analog ICs provide *evaluation boards* usually at a nominal cost. These boards allow customers to evaluate ICs without constructing their own prototypes. Regardless of the product, the manufacturer has taken proper precautions regarding grounding, layout, and decoupling to ensure optimum device performance. Where applicable, the evaluation PCB artwork is usually made available free of charge, should a customer wish to copy the layout directly or make modifications to suit an application.

General Purpose Op Amp Evaluation Board from the Mid-1990s

Evaluation boards can be either dedicated to a particular IC, or they can also be general purpose. With op amps the most universal linear IC, it is logical that evaluation boards be developed for them, to aid easy applications. However, it is also important that a good quality evaluation board avoid the parasitic effects discussed above. An example is the general purpose dual amplifier evaluation board of in Figure 9.190 (see Reference 10).

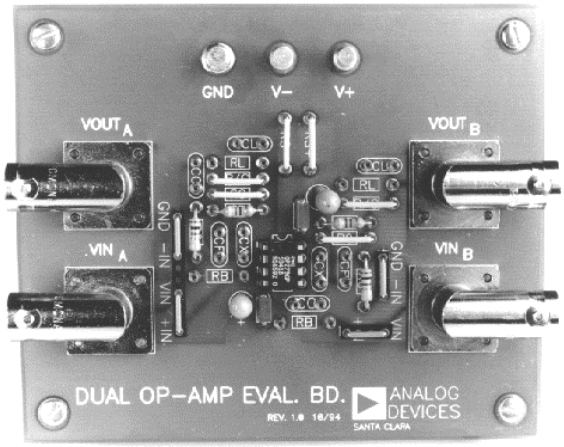


***Figure 9.190:** A Mid-1990s General Purpose Op Amp Evaluation Board Allowed Fast, Easy Configuration of Low Frequency Op Amps in DIL Packages*

This board uses pin sockets for any standard dual op amp pinout device, and a flexible set of component jumper locations allows it to be setup for inverting or non-inverting amplifiers. Various gains can be configured by choice of the component values, in either ac- or dc-coupled configurations.

The card design provides signal coupling via BNC connectors at input and output. It also uses external lab power supplies, which are wired to the lug terminals at the top. The card does however contain local supply voltage decoupling and bypassing components.

These general purpose boards are intended for medium to high precision uses at frequencies below 10 MHz, with moderate op amp input currents. For higher operating speeds, a dedicated, device-specific evaluation board is a better choice.

Dedicated Op Amp Evaluation Boards

In high speed/high precision ICs, special attention must be given to power supply decoupling. For example, fast slewing signals into relatively low impedance loads produce high speed transient currents at the power supply pins of an op amp. The transient currents produce corresponding voltages across any parasitic impedance that may exist in the power supply traces. These voltages, in turn, may couple to the amplifier output, because of the op amp's finite power supply rejection at high frequencies.

The AD8001 high speed current-feedback amplifier is a case in point, and a dedicated evaluation board is available for it. A bottom side view of this SOIC board is shown in

Figure 9.181. A triple decoupling scheme was chosen, to ensure a low impedance ground path at all transient frequencies. Highest frequency transients are shunted to ground by dual 1000-pF/0.01-µF ceramic chip capacitors, located as close to the power supply pins as possible to minimize series inductance and resistance. With these surface mount components, there is minimum stray inductance and resistance in the ground plane path. Lower frequency transient currents are shunted by the larger 10-µF tantalum capacitors.

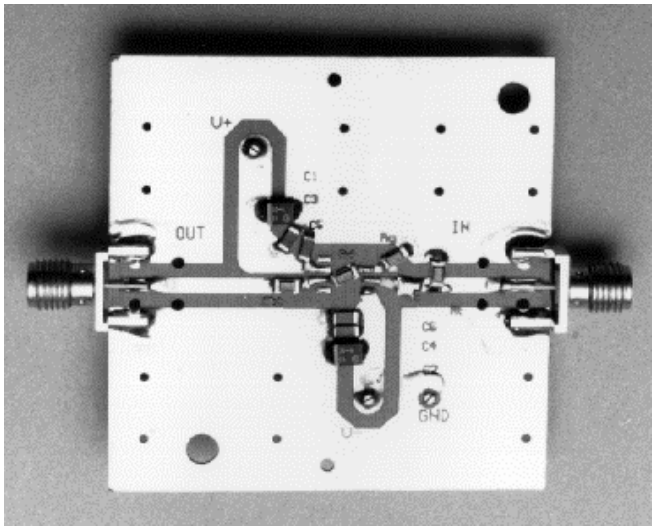


Figure 9.181: *A High Speed Op Amp Such as the AD8001 Requires a Dedicated Evaluation Board With Suitable Ground Planes and Decoupling (Bottom View)*

The input and output signal traces of this board are 50-Ω microstrip transmission lines, as can be noted towards the right and left. Gain-set resistors are chip-style film resistors, which have low parasitic inductance. These can be seen in the center of the photo, mounted at a slight diagonal.

Note also that there is considerable continuous ground plane area on both sides of the PCB. Plated-through holes connect the top and bottom side ground planes at several points, in order to maintain lowest possible impedance and best high frequency ground continuity.

Input and output connections to the card are provided via the SMA connectors as shown, which terminate the input/output signal transmission lines. The board's power connection from external lab supplies is made via solder terminals, which are seen at the ends of the broad supply line traces.

Some of these points are more easily seen in a topside view of the same card, which is shown in Figure 9.182. This AD8001 evaluation board is a non-inverting signal gain stage, optimized for lowest parasitic capacitance. The cutaway area around the SOIC outline of the AD8001 provides lowest stray capacitance, as can be noted in this view.

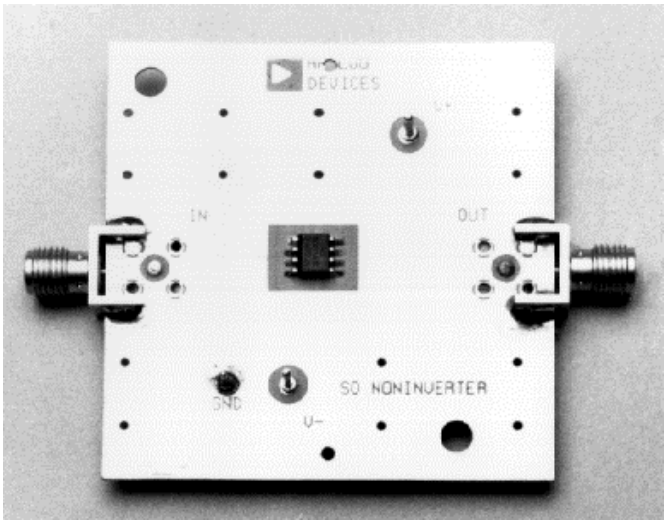


Figure 9.182: *The AD8001 Evaluation Board Uses a Large Area Ground Plane as well as Minimal Parasitic Capacitance (Top View)*

In this view is also seen the virtually continuous ground plane and the multiple vias, connecting the top/bottom planes.

Data Converter Evaluation Boards

A well designed manufacturers' evaluation board is a powerful tool that can greatly simplify the integration of an ADC or DAC into a system. Probably the best feature of an evaluation board is that its layout is designed to optimize the performance of the data converter. Analog Devices provides a complete electrical schematic and parts list as well as a PC board layout of its evaluation boards on the data sheet for most ADCs and DACs. Each layer of the multilayer board is also shown, and Analog Devices will supply the CAD layout files (Gerber format) for the board if needed. Many system level problems related to layout can be avoided simply by studying the evaluation board layout and using it as a guide in the system board layout—perhaps even copying critical parts of the layout directly if needed.

Evaluation boards typically have input/output connectors for the analog, digital, and power interfaces to facilitate interfacing with external test equipment. Any required support circuitry such as voltage references, crystal oscillators for clock generation, etc., are generally included as part of the board.

Many modern data converters have a considerable amount of on-chip digital logic for controlling various modes of operation, including gain, offset, calibration, data transfer, etc. These options are set by loading the appropriate words into internal control registers, usually via a serial port. In some converters, especially sigma-delta ADCs, just setting the basic options requires considerable knowledge of the internal control registers and the interface. For this reason, most ADC/DAC evaluation boards have interfaces (either parallel, serial, or USB) and software to allow easy menu-driven control of the various internal options from an external PC. In many cases, configuration files created in the evaluation software can be downloaded into the final system design.

Figure 9.183 shows the evaluation board for the AD7730 24-bit bridge transducer sigma-delta ADC. This ADC has an on-chip PGA and is designed to interface directly to a variety of bridge transducers. A load cell with a 10-mV full-scale output can be connected directly to the ADC input, and the output is read by the PC via the parallel port interface. The evaluation board software allows the system designer to see the effects of sample rate, gain, filter bandwidth, and output data averaging on the overall effective resolution. The software also provides histogram displays for direct evaluation of system noise.

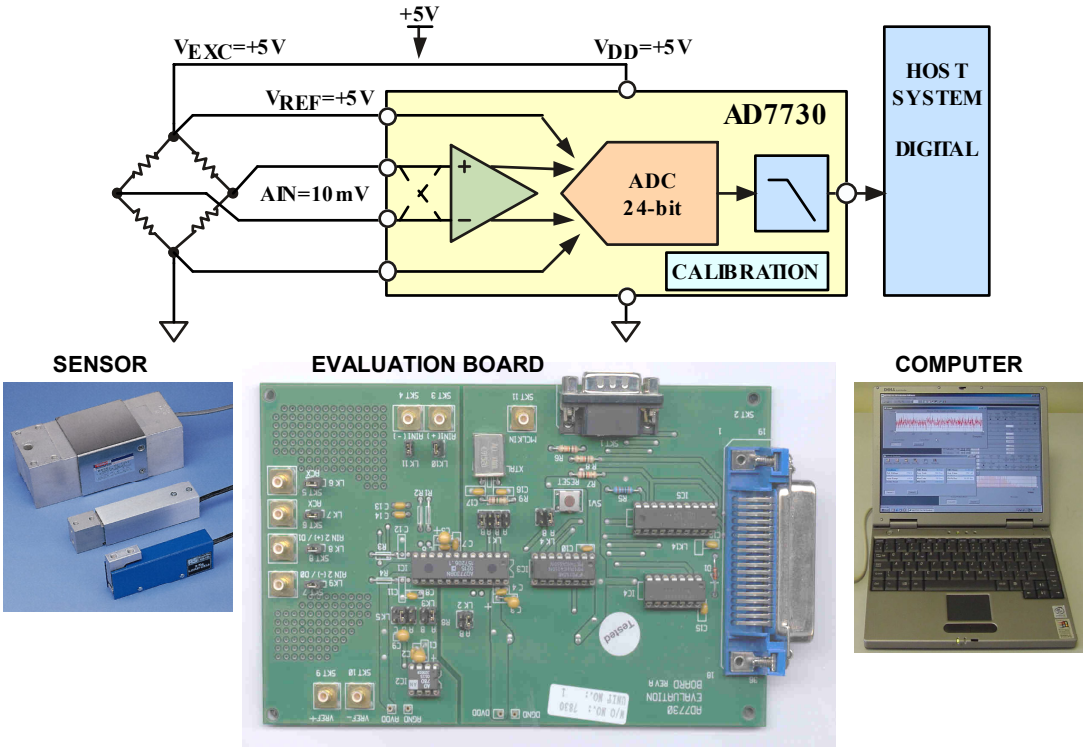


Figure 9.183: *AD7730 Measurement ADC Evaluation System*

Figure 9.184 shows the evaluation board for the AD5535 32-channel 14-bit high voltage DAC. The evaluation board interfaces with an external PC via a parallel port connector. The software provided with the board allows data to be easily loaded into the individual DAC registers via the 3-wire serial interface.

Figure 9.185 shows an ADC evaluation board for the AD7450 12-bit 1-MSPS ADC connected to an Evaluation/Control board. The ADC evaluation board (right side of diagram) is product-specific, but the evaluation/control board interfaces to a variety of ADC evaluation boards and has an on-board 16-bit buffer memory and control logic which interfaces to a PC via the parallel port. The software provided includes an FFT routine which allows evaluating the ADC under dynamic conditions. The evaluation/control board can handle ADCs with sampling rates up to several MHz.

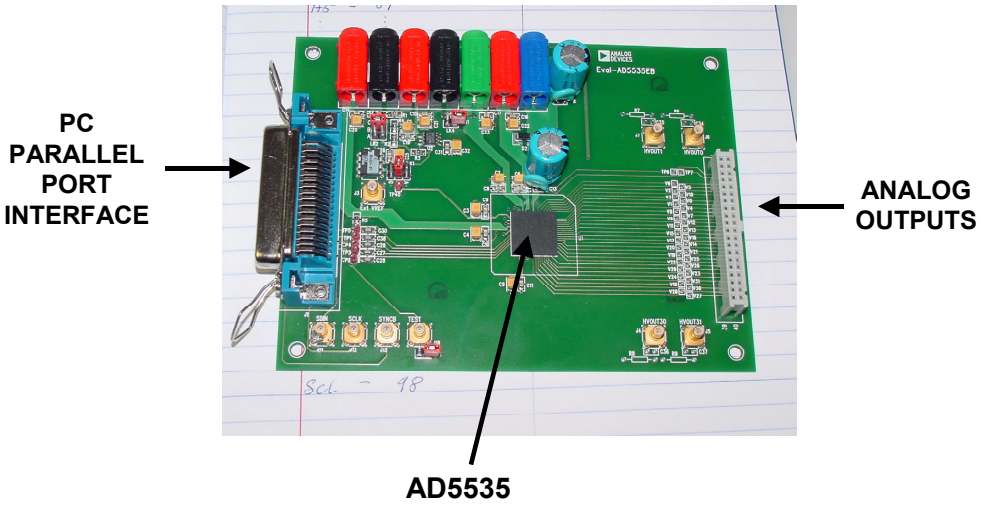


Figure 9.184: *AD5535 32-Channel, 14-Bit, 200V Output DAC Evaluation Board*

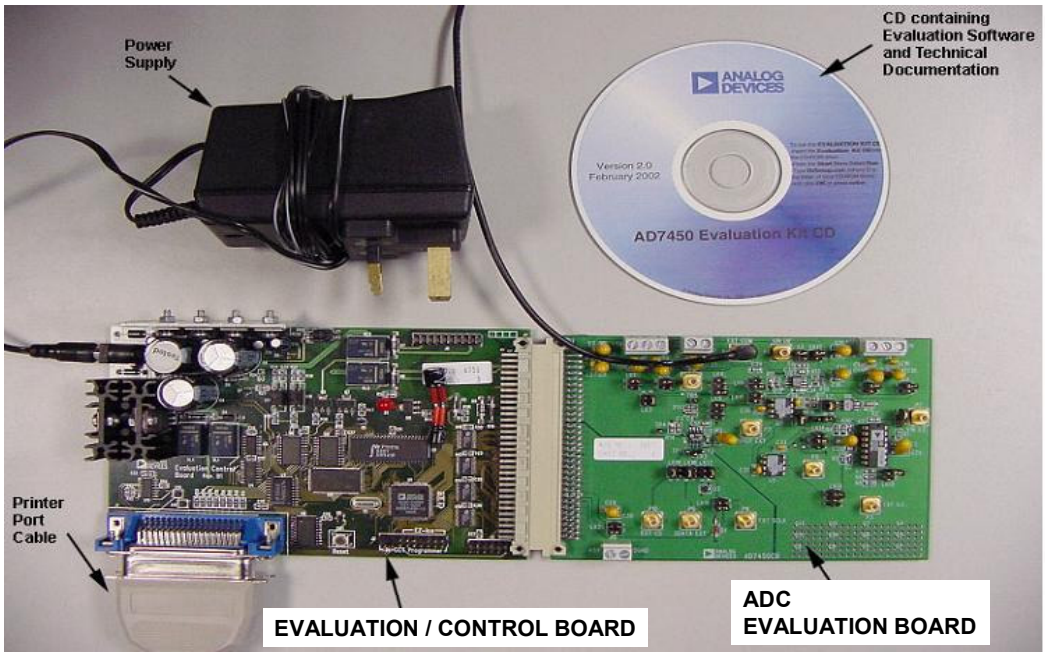


Figure 9.185: *Evaluation/Control Board and ADC Evaluation Board for ADCs*

Figure 9.186 shows Analog Devices' high-speed ADC FIFO evaluation kit which interfaces to a variety of high-speed ADC evaluation boards, such as the AD9430 12-bit, 210-MSPS ADC. The FIFO evaluation kit includes a memory board to capture blocks of data from the ADC as well as ADC Analyzer software. The FIFO board can be connected to the parallel port of a PC through a standard printer cable and used with the ADC Analyzer software to quickly evaluate the performance of the high speed ADC. The FIFO board contains two 32K, 16-bit wide FIFOs, and data can be captured at clock rates up to 133 MSPS on each channel. Memory upgrades are available to increase the size of the FIFO to 64K, 132K, or 256K. Two versions of the FIFO are available—one version is used with dual ADCs or ADCs with demultiplexed digital outputs, and the other version

is used with single-channel ADCs. Users can view the FFT output and analyze SNR, SINAD, SFDR, THD, and harmonic distortion information.

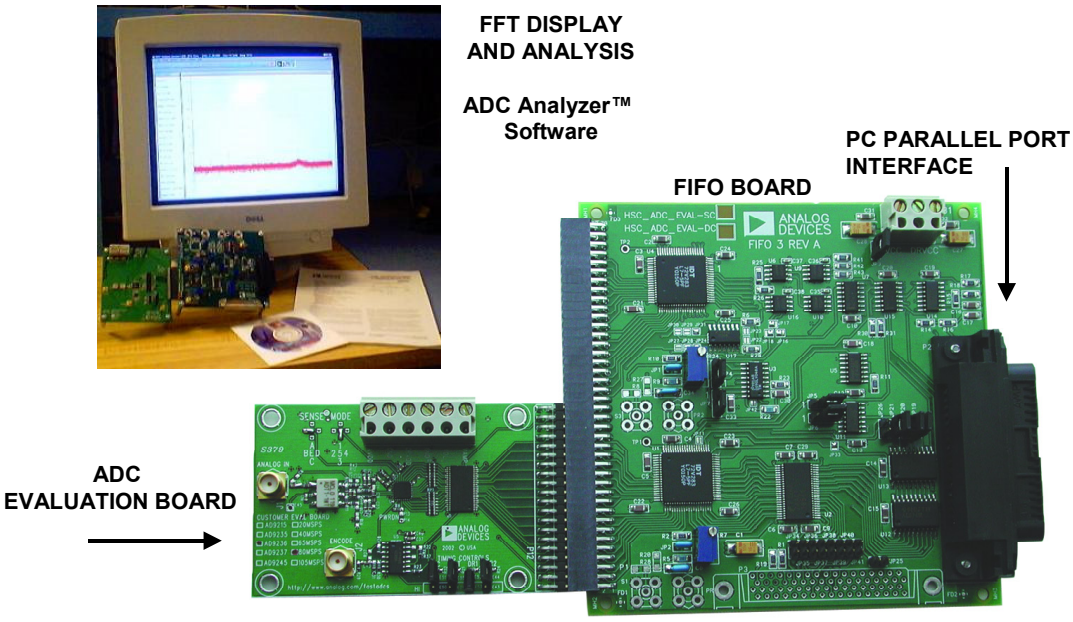


Figure 9.186: *Analog Devices' High Speed ADC FIFO Evaluation Kit*

Summary

The prototyping techniques described earlier in this section are quite useful for ICs which are in DIP packages, and it is well worth the effort to prototype at least some of the critical analog circuitry before going to a final board layout. However, modern high performance ADCs and DACs are often provided in small surface mount packages which do not lend themselves to simple prototyping techniques. In the system, multilayer PC boards are required which further complicates the prototyping process.

In many cases, the only effective prototype for high performance analog systems is an actual PC board layout, especially if a multilayer is required in the final design. Evaluation boards are not only useful in the initial evaluation phases, but their layouts can be used as guides for the actual system board layout.

Successful integration of a high performance data converter into a system therefore requires excellent support from the manufacturer as well as care and attention to detail by the user.

REFERENCES:
9.8 BREADBOARDING AND PROTOTYPING

1. Jim Williams, "High Speed Amplifier Techniques," Linear Technology AN-47, August, 1991.

2. Robert A. Pease, **Troubleshooting Analog Circuits**, Butterworth-Heinemann, 1991, ISBN 0-7506-9184-0.

3. Vector Electronic Company, 12460 Gladstone Ave., Sylmar, CA 91342, Tel. 818-365-9661.

4. Wainwright Instruments Inc., 69 Madison Ave., Telford, PA, 18969-1829, (215) 723-4333, http://www.rdi-wainwright.com/

5. Wainwright Instruments GmbH, Widdersberger Strasse 14, DW-8138 Andechs-Frieding, Germany. +49-8152-3162.

6. PADS Software, Advanced CAM Technologies, Inc., 16450 Los Gatos Blvd., Suite 110, Los Gatos, CA 95032, http://www.ecam.com/

7. ACCEL Technologies, Inc., 17140 Bernardo Center Drive, Suite 100, San Diego, CA 92128, http://www.acceltech.com/

8. LPKF Laser & Electronics, 28220 SW Boberg Rd., Wilsonville, OR 97020, 800-345-LPKF or (503) 454-4200, http://www.lpkfcadcam.com

9. T-Tech, Inc., 5591-B New Peachtree Road, Atlanta, GA, 34341, 800 370-1530 or (770) 455-0676, http://www.T-Tech.com

10. Adolfo Garcia, "Evaluation Boards for Single, Dual and Quad Operational Amplifiers," **Analog Devices AN398**, January 1996.

NOTES: